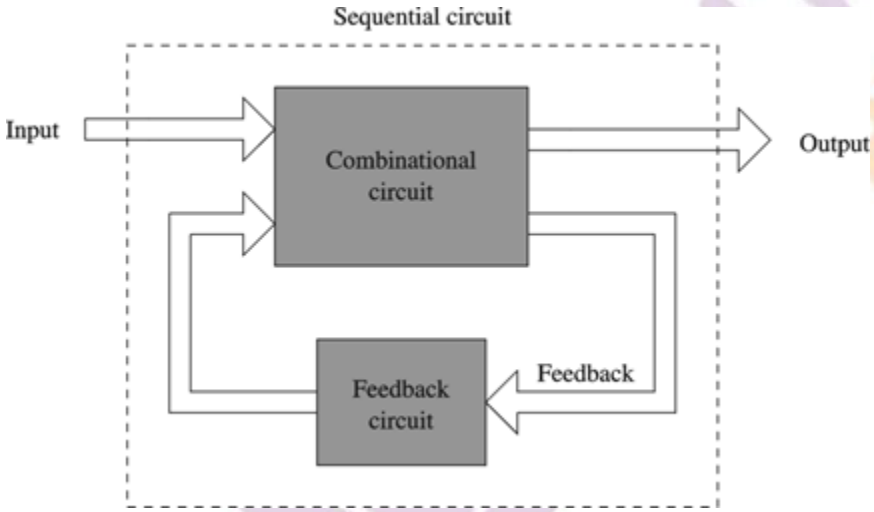
Sequential Circuits (Phase-1) Study Notes for GATE & Computer Science Engineering Exams

Sequential circuits form a fundamental building block in the field of digital electronics and play a significant role in the Graduate Aptitude Test in Engineering (GATE) and Computer Science Engineering exams. Understanding the principles and concepts behind sequential circuits is crucial for success in these exams.

Here we have provided comprehensive study notes for Sequential Circuits (Phase-1), focusing on key concepts and important topics to help in your GATE preparation.

In a sequential logic circuit, the output of the circuit is dependent upon the present inputs as well as the past inputs and outputs.



A sequential circuit is of two types.

- **Synchronous Sequential Circuit:** Change in input signals can affect memory elements only upon activation of clock signals.
- **Asynchronous Sequential Circuit:** Change in input signals can affect memory elements at any instant of time. These are faster than the synchronous circuit.

Flip Flops:

- It is a one-bit memory cell which stores the 1-bit logical data (logic 0 or logic 1).
- It is a basic memory element.
- The most commonly used application of flip flops is in the implementation of a feedback circuit.

- As a memory relies on the feedback concept, flip flops can be used to design it.
- In the synchronous sequential circuit, Memory elements are clocked flip flops and generally edge triggered.
- In the asynchronous sequential circuit, Memory elements are unclocked flip flops/time delay elements which are generally level triggered.
- Flip flop circuit is also known as bistable multivibrator or latch because it has two stable states (1 state, 0 state).

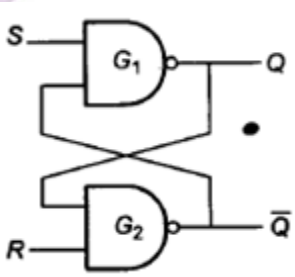
There are mainly four types of flip flops that are used in electronic circuits.

- S-R Flip Flop (Basic Flip Flop)
- Delay Flip Flop (D Flip Flop)
- J-K Flip Flop
- T Flip Flop

Basic SR Flip Flop:

- The Set-Reset (SR) flip flop is designed with the help of two NOR gates or two NAND gates.
- SR Flip Flop is also called as SR latch.

SR Latch Implementation Using NAND Gates

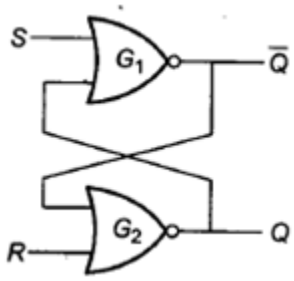


Logic diagram of SR latch using NAND gates

S	R	Q
0	0	Invalid
0	1	1
1	0	0
1	1	Previous state

Truth Table of Logic Diagram

SR Latch Using NOR Gates:



Logic diagram of SR latch using NOR gates

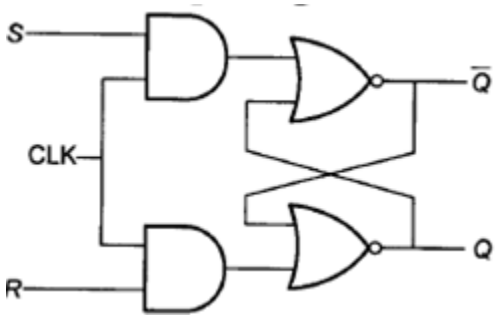
S	R	Q
0	0	Previous state
0	1	1
1	0	0
1	1	Invalid

Truth Table of Logic Diagram

Clocked SR Flip Flop Implementation using NAND Gates

It is also called a Gated S-R flip flop. The problem with S-R flip flops using NOR and NAND gate is the invalid state. This problem can be overcome by using a biostable SR flip-flop that can change outputs when certain invalid states are met, regardless of the condition of either the Set or the Reset inputs.

- **SR Flip Flop Using NOR Gates:**



Logic diagram of SR flip flop using NOR gates

Clock	S	R	Q
0	×	×	Q_n
1	0	0	$Q_n \rightarrow$ Hold
1	0	1	$0 \rightarrow$ Hold
1	1	0	$1 \rightarrow$ Hold
1	1	1	Invalid

Also Read: Combinational and Sequential Difference

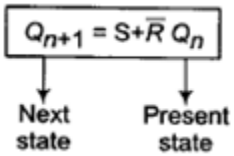
Truth Table of SR Flip Flop

With both S=1 and R=1, the occurrence of a clock pulse causes both outputs to momentarily go to 0. When the pulse is taken away then, the state of the flip-flop is indeterminate, depending on whether the set or reset input of the flip-flop remains a 1 longer than the transition to 0 at the ending of the pulse.

Characteristic Table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	×
1	1	1	×

Characteristic equation of SR flip flop



Excitation Table:

Q_n	Q_{n+1}	S	R
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

GATE Computer Science Engineering Revision Sheet and Formulae

JK Flip Flop

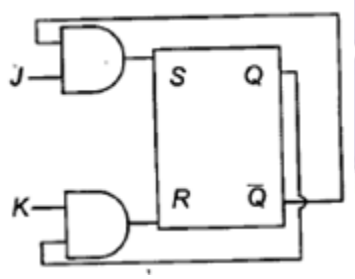
A JK flip-flop eliminates indeterminate state of the SR type. Inputs J and K behave same like inputs S and R to set and clear the flip-flop (In JK flip-flop, the letter J is for set and the letter K is for clear).

When logic 1 inputs are applied to J also K simultaneously, the flip-flop switches to its complement state. If Q=1, it switches to Q=0 and vice versa from 0 to 1.

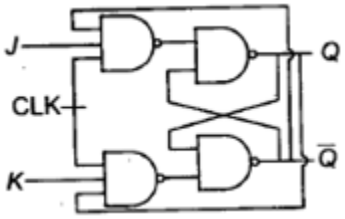
- **JK flip flop using SR flip flop**

S = JQ'

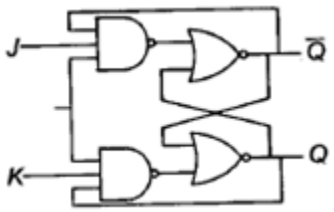
R = KQ



- JK flip flop using NAND latch



- JK flip flop using NOR latch



Characteristic Table

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table

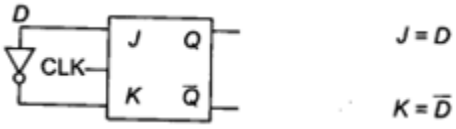
Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

- **Characteristic equation for JK flip flop:**

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

D-Flip Flop: D flip flop is also known as Transparent latch, Delay flip flop or data flip flop. The D input goes straightaway into the S (J) input and the complement of the D input goes to the R (K) input.

- The D-flipflop has only a single data input (D).
- If D = 1, the flip-flop is switched to the set state (unless it was already set).
- If D = 0, the flip-flop switches to the clear state.



Truth Table

Clock	D	Q_{n+1}
0	×	Q_n ← Memory
1	0	0 ← Reset
1	1	1 ← Set

Characteristic Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

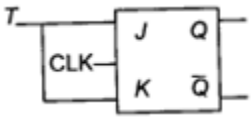
Characteristic equation for D-flop flop:

$Q_{n+1} = D$

T – Flip Flop

- The T flip-flop is a single input version of the JK flip-flop where T is connected to both J and K inputs directly.
- When T = 0, the flip flop enters into **Hold** mode, which means that the output Q is kept the same as it was before the clock edge.

- When T = 1, the flip flop enters into **Toggle** mode, which means the output Q is negated after the clock edge, compared to the value before the clock edge.



Truth Table

Clock	T	Q_{n+1}
0	×	$Q_n \rightarrow$ Memory
1	0	$Q_n \rightarrow$ Hold
1	1	$Q_n \rightarrow$ Toggle

Characteristic Table

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

- **Characteristic equation of T-Flip Flop:**

$Q_{n+1} = T \oplus Q_n$

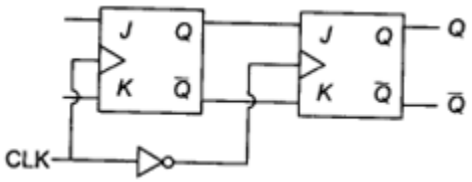
- **Race Around Condition:**
  - The race around condition will occur in JK flip flop when J = *K* = 1 and $t_{pd\ (FF)} < t_{pw.}$

- To avoid race around condition.

$t_{pw} < t_{pd\ (FF)} < T_{CLK}$

Master Slave (MS) Flip Flop

- A master-slave flip-flop is constructed from two separate flip-flops. One circuit serves as a **master** and the other as a **slave**. Input clock is applied to master and Inverted clock applied to slave.



- In Master Slave flip flop output is changed only when slave output is changing.
- The master flip-flop is enabled on the positive edge of the clock pulse and the slave flip-flop is disabled by the inverter.
- The information at the external J and K inputs is transmitted to the master flip-flop.
- When the pulse returns to 0, the master flip-flop is disabled and the slave flip-flop is enabled. The slave flip-flop then goes to the same state as the master flip-flop.
- Master is level triggered, and Slave is edge triggered
- No race around condition occurs in Master Slave flip flops.
- It stores only one bit.

In these study notes, we've covered the basics of sequential circuits. Remember to practice solving problems and implement the concepts learned to strengthen your understanding.

Thanks!

BYJU'S Exam Prep - The Most Comprehensive App!