Digital Electronics GATE Questions

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1. The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

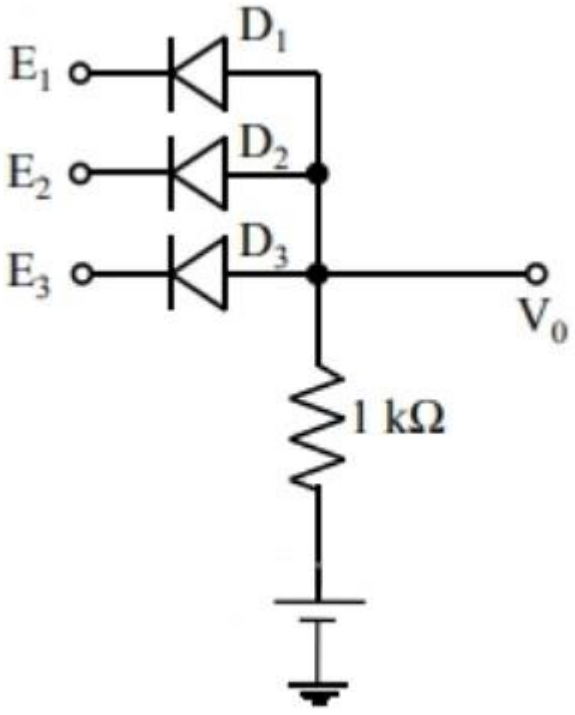
   (GATE ECE 2016 Set 3)

   a. 4
   b. 5
   c. 6
   d. 7

   Answer (a)

2. In the circuit shown, diodes and are ideal, and the inputs and are “0 V” for logic ‘0’ and “10 V” for logic ‘1’. What logic gate does the circuit represent?

   (GATE ECE 2015 Set 3)



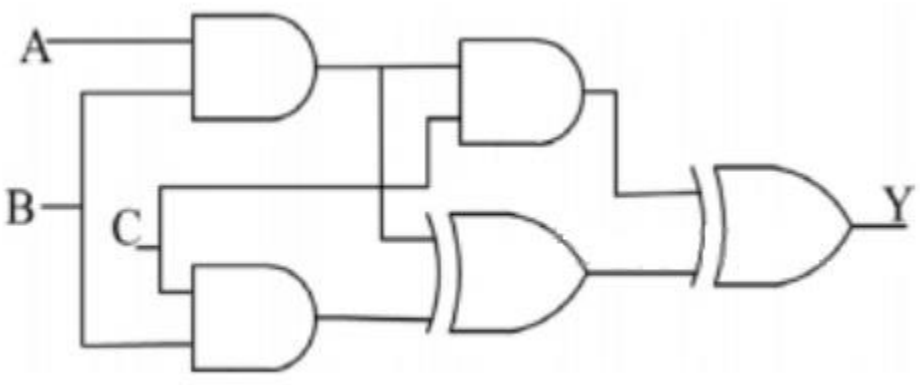
   a. 3-input OR gate
   b. 3-input NOR gate
   c. 3-input AND gate

d. 3-input XOR gate

Answer (c)

3. The output of the combinational circuit given below is

(GATE ECE 2016 Set 1)



a. A+B+C
b. A(B+C)
c. B(+A)
d. C(A+B)

Answer (c)

4. A bulb in a staircase has two switches, one switch being on the ground floor and the other one on the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches, irrespective of the state of the other switch. The logic of switching of the bulb resembles.

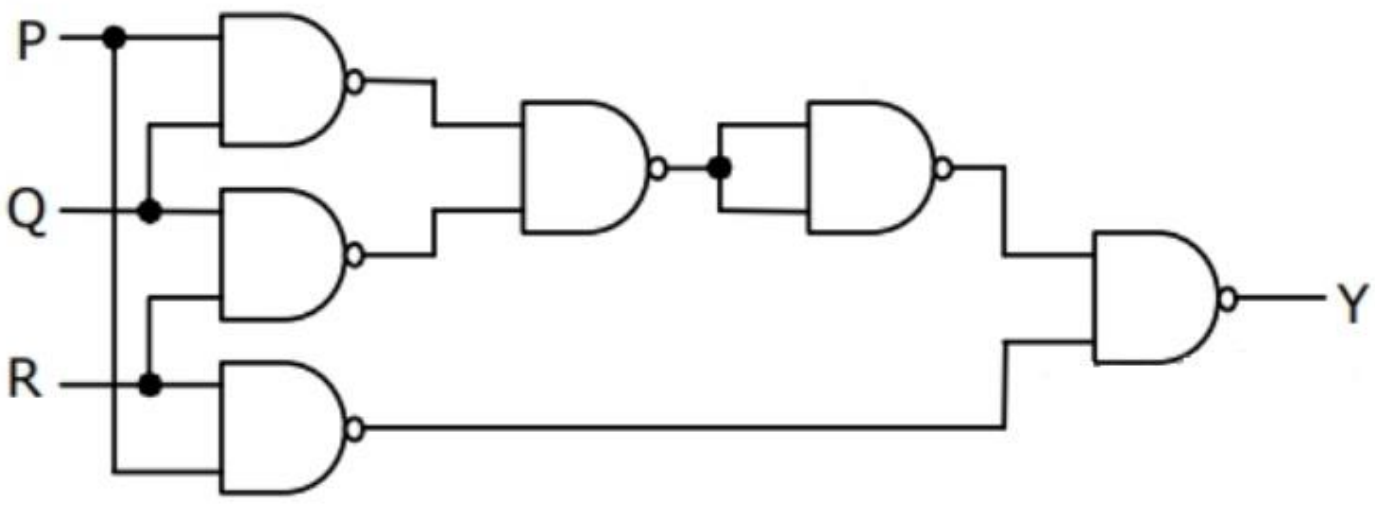
(GATE ECE 2011)

a. An AND gate
b. An OR gate
c. An XOR gate
d. A NAND gate

Answer (c)

5. The output Y in the circuit below is always '1' when

(GATE ECE 2011)



a. Two or more of the inputs P, Q, R are '0'
b. Two or more of the inputs P, Q, R are '1'
c. Any odd number of the inputs P, Q, R is '0'
d. Any odd number of the inputs P, Q, R is '1'

Answer (b)

6. Consider a four bit D to A converter. The analog values corresponding to digital signals of values 0000 and 0001 are 0 V and 0.0625 V, respectively. The analog value (in Volts) corresponding to the digitals signal 1111 is _____

(GATE ECE 2002)

a. 0.93
b. 0.95
c. 0
d. 1

Answer (a)

7. The number of comparators required in a 3-bit comparator type ADC is

(GATE ECE 2002)

a. 2
b. 3
c. 7
d. 8

Answer (c)

8. The number of comparators in 4-bit flash ADC is

(GATE ECE 2000)

a. 4
b. 5
c. 15
d. 16

Answer (c)

9. A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle, GREEN is turned on for 70 seconds, YELLOW is turned on for 5 seconds and the RED is turned on for 75 seconds. This traffic light has to be implemented using a finite state machine (FSM). The only input to this FSM is a clock of 5 second period. The minimum number of flip-flops required to implement this FSM is _____

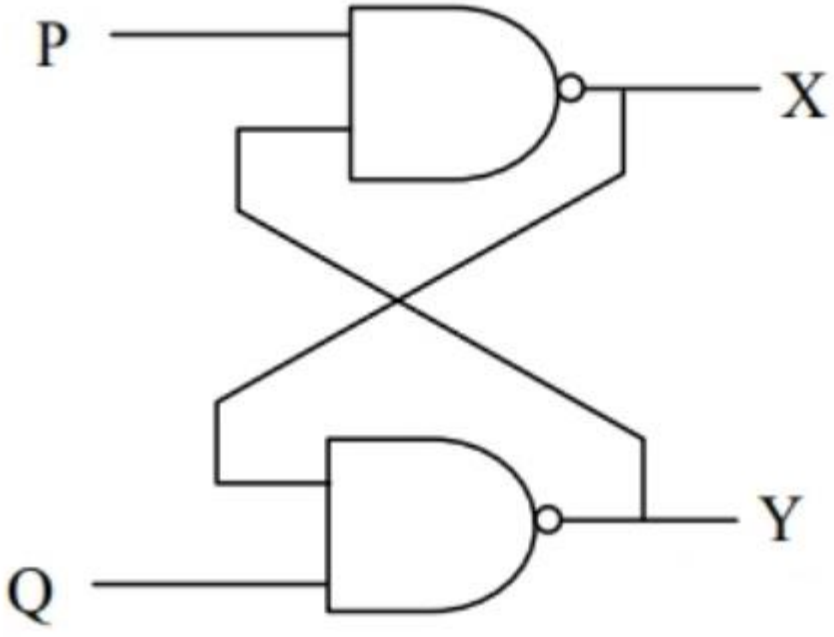
(GATE ECE 2018)

a. 5
b. 7
c. 10
d. 15

Answer (a)

10. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = "0". If the input condition is changed simultaneously to P = Q = "1", the outputs X and Y are

(GATE ECE 2017 Set 1)



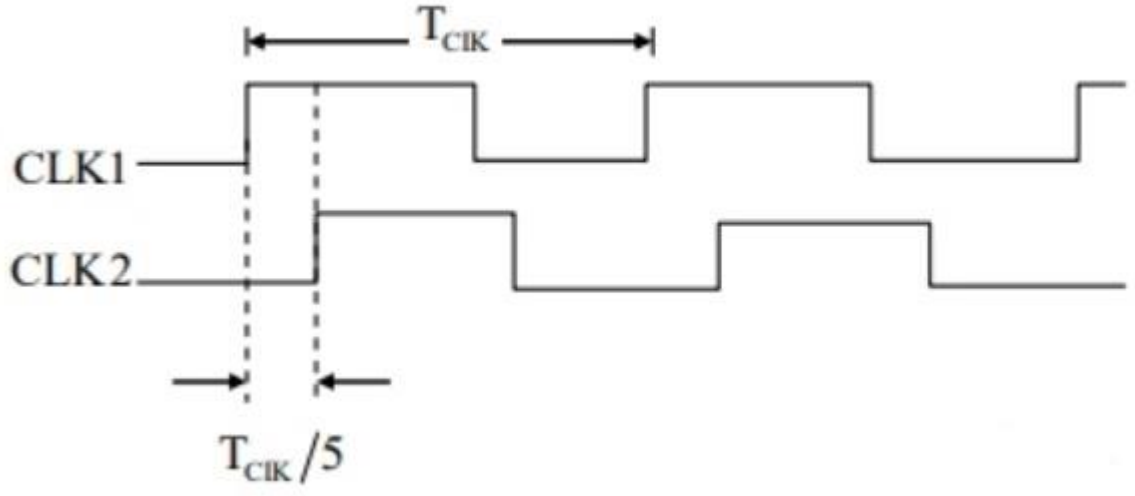
a. X = '1', Y ='1'
b. Either X = '1', Y = '0' or X ='0', Y = '1'
c. Either X = '1', Y = '1' or X ='0', Y = '0'

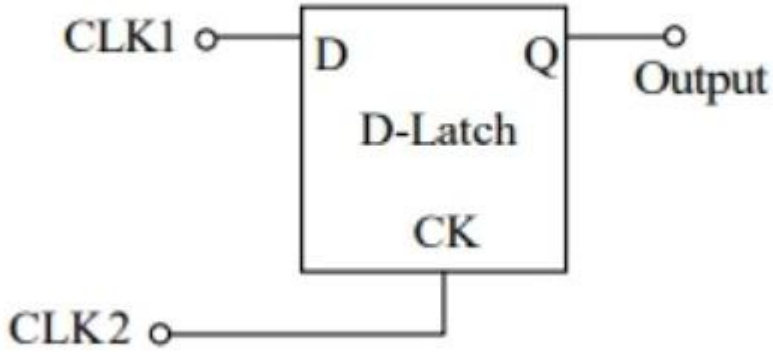
d. X = '0', Y ='0'

Answer (b)

11. Consider the D-Latch shown in the figure, which is transparent when its clock input CK is high and has zero propagation delay. In the figure, the clock signal CLK1 has a 50% duty cycle and CLK2 is a one-fifth period delayed version of CLK1. The duty cycle at the output latch in percentage is _____

(GATE ECE 2017 Set 1)



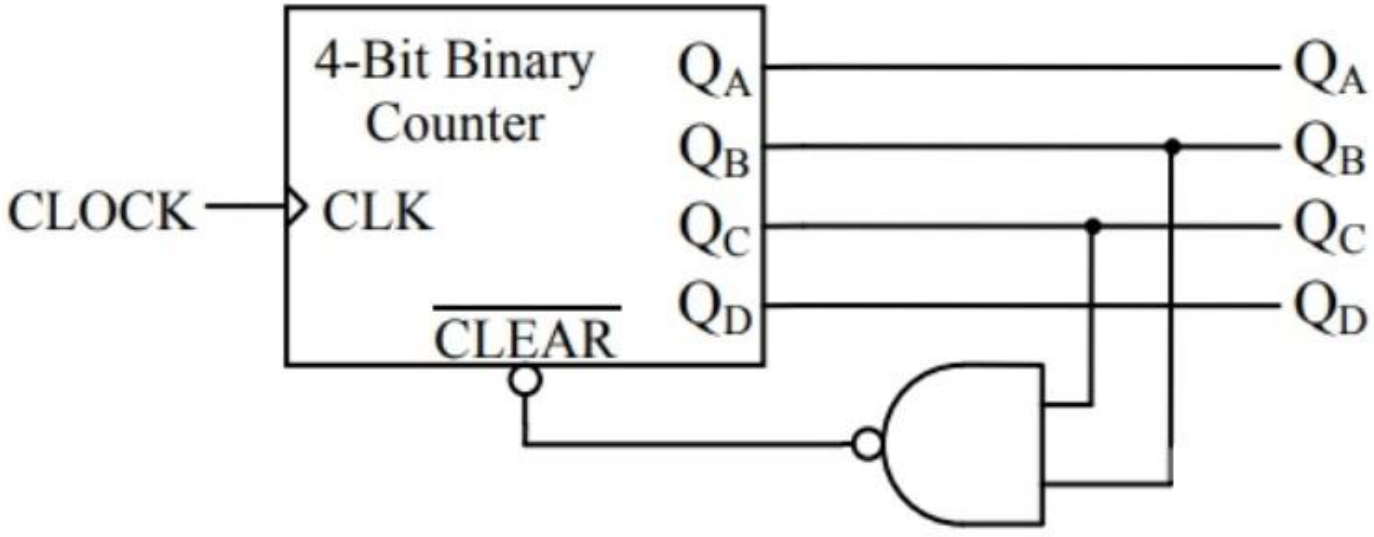


a. 25
b. 30
c. 35
d. 40

Answer (b)

12. A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure. The value of n is _____

(GATE ECE 2015 Set 2)

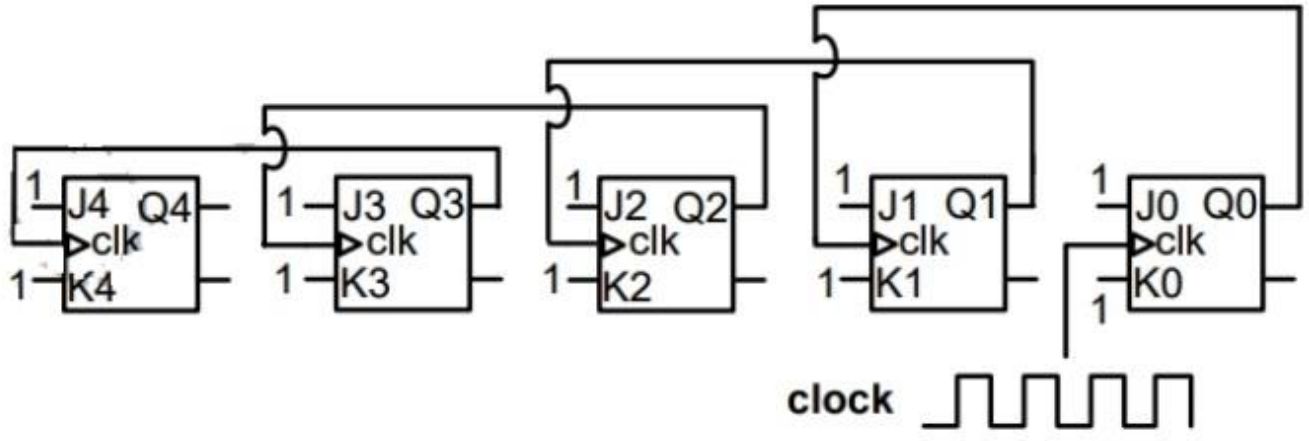


a. 7
b. 10
c. 15
d. 20

Answer (a)

13. Five JK flip – flops are cascaded to form a circuit shown in figure. The clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at Q_3 is _____

(GATE ECE 2014 Set 1)



a. 62.5
b. 66
c. 67.67
d. 70

Answer (a)

14. In a DRAM,

(GATE ECE 2017 Set 2)

a. Periodic refreshing is not required
b. Information is stored in a capacitor
c. Information is stored in a latch
d. Both read and write operations can be performed simultaneously

Answer (b)

15. A 16 Kb (=16,384 bit) memory array is designed as a square with an aspect ratio of one (number of rows is equal to the number of columns). The minimum number of address lines needed for the row decoder is _____

(GATE ECE 2015 Set 1)

a. 10
b. 7
c. 5
d. 1

Answer (b)

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