1. Identify the combinational logic circuit(s) from the following list:

   I. Full adder

   II. J-K flip-flop

   III. Counter

   A. II only B. III only

   C. II and III D. I only

Ans. D

Sol. The combinational circuits are:

   I. Full adder

   II. Full subtractor

   III. Multiplexers

   IV. De-multiplexers

   V. Encoders

   VI. Decoders

2. For an 8085 microprocessor, the value of (the number of maskable interrupts) – (the number of non-maskable interrupts) is:

   A. 4 B. 3

   C. 2 D. 1

Ans. B

Sol. For an 8085 microprocessor, the value of difference of the number of maskable interrupts to the number of non-maskable interrupts is 3.

3. Which of the following analog-to-digital converters takes maximum time (slowest)?

   A. Counting type B. Successive approximation type

   C. Integrating type D. Parallel comparator (flash) type

Ans. C

Sol. Integrating type ADC is the slowest converter whereas the Flash type ADC is the fastest one.

4. The reduced state table of a sequential machine has 7 rows. What is the minimum number of flip flops needed to implement the machine?

   A. 0 B. 2

   C. 3 D. 7

Ans. C

Sol. Number of rows $\leq 2^n$

   n = number flip flops

   $7 \leq 2^n$

   n = 3

5. In a J-K flip-flop, if $J = \bar{K}$, then it acts as a/an:

A. T flip-flop B. D flip-flop

C. RS flip-flop D. Decoder

Ans. B

Sol. In a J-K Flip flop, if $J = \bar{K}$, then it acts as a D Flip flop.

6. A static memory stores its data in:

A. Flip-flops B. Inductors

C. Capacitors D. Resistors

Ans. A

Sol. Static random-access memory (static RAM or SRAM) is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit.

7. Convert (0.7854)10 to binary.

A. $(0.1010)_2$ B. (0.1110)2

C. $(0.1100)_2$ D. (0.1101)2

Ans. C

Sol. Conversion of Decimal to Binary of floating numbers:

(0.7854)10 = ?

0.7854 x 2 = 1

0.5708 x 2 = 1

0.1416 x 2 = 0

0.2832 x 2 = 0

$(0.7854)_{10} = (0.1100)_2$

8. A register capable of incrementing and/or decrementing its contents.

A. Counter B. Decoder

C. Multiplexer D. Demultiplexer

Ans. A

Sol. Counter is a sequential circuit which is used to count the number in ascending or descending order of its contents in the registers or flip flops.

9. _____ is also known as Inverter.

A. NOT Gate B. OR Gate

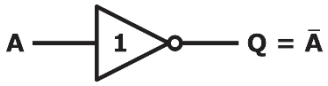
C. NAND Gate D. AND Gate

Ans. A

Sol. The logic NOT function output is true when its single input is false, and false when its single input is true.

NOT Function Truth Table

Switch	Output
1	0
0	1
Boolean Expression	Not-A or $\overline{A}$



Inverter or NOT Gate

10. Number of comparators required for an 8 bit flash ADC is:

A. 8 B. 16

C. 255 D. 256

Ans. C

Sol. Number of comparators required for 'n' bit flash ADC is = $2^n - 1$

n: number of bits

Here, n =8

Number of comparators required = $2^8 - 1 = 256 - 1 = 255$

11. A 4-bit-16 ripple counter uses J-K flip-flop. If the propagation delay of each flip-flop is 50 nanoseconds, the maximum clock frequency that can be used is equal to:

A. 20 MHz B. 10 MHz

C. 8 MHz D. 5 MHz

Ans. D

Sol. Prepogation delay of each flip flop = 50 nano seconds

As 4 bit ripple counter is given

Total prepogation delay of fever flip flops = 4 × 50 = 200 nano seconds

$\therefore$ Maximum clock frequency = $\frac{1}{T} = \frac{1}{200 \text{ nano seconds}}$

f = 5 MHz

12. A single binary digit is called:

A. Byte B. Bit

C. Data D. Logic

Ans. B

Sol. A binary digit, or bit, is the smallest unit of information in a computer. It is used for storing information and has a value of true/false, or on/off. An individual bit has a value of either 0 or 1, which is generally used to store data and implement instructions in groups of bytes.

13. Without any additional circuitry, an 8:1 MUX can be used to obtain:

A. Some but not all Boolean functions of 3 variables

B. All function of 3 variables but none of 4 variables

C. All functions of 3 variables and some but not all of 4 variables

D. All functions of 4 variables

Ans. C

Sol. For 8:1 Mux ⇒ 3 select lines, 8 input lines and 1 output line.

So, 3 variable function can be implemented by 8:1 Mux(By connecting corresponding min terms to 1 and remaining to 0)

Now, in case of 4 variables, there are only 3 select lines, but we need to represent 4 variables. So, output should also depend on 4th variable. Also, an inverted variable input is also there. So, not all functions having 4 variables can be represented.

14. The complement of AB+BC'+CD' is:

A. A'CD + B'C' + B'D

B. A'C' + BC + AB'D'

C. AC + BC + ABD

D. A'C' + B'C' + A'B'D'

Ans. A

Sol. AB+BC'+CD' ⇒ $\overline{AB+BC'+CD'}$ ⇒ (B' +C) (A'+B') (C'+D) ⇒ (A'B' + B' + A'C + B'C) (C'+D)

⇒ (B' + A' C) (C' + D) ⇒ B' C' + B' D + A' CD.

So option (a) is the answer.

15. The following expression when simplified will become XY(X' YZ + X' Y' Z' + X Y' Z)

A. 0

B. 1

C. – 1

D. X

Ans. A

Sol. Multiplying inside bracket we get: XX' YYZ + XX' YY' Z' + XX YY' Z ⇒ 0 + 0 + 0 ⇒ 0

16. In an unclocked R-S flip flop made of NOR gates, the forbidden input condition is:

A. R = 0, S = 0

B. R = 1, S = 0

C. R = 0, S = 1

D. R = 1, S = 1

Ans. D

Sol. The truth table for a RS flip flop is given below:

S	R	Q	State
0	0	Previous State	No change
0	1	0	Reset
1	0	1	Set
1	1	?	Forbidden

From the truth table it is clear that answer will be option (d)

17. A 339 IC is an example of a fourteen-pin DIP that can be made to function as a _____:

A. Comparator
B. 555 timer
C. D to A converter
D. Ladder network

Ans. A

Sol. LM339 is basically a comparator IC that has four comparators inbuilt inside it. It compares the two input voltages applied to its input terminals, and its output is a digital voltage that indicates which signal among the two input signals are greater.

18. In 8085 microprocessor with memory mapped I/O which of the following is true?

A. I/O devices have 16 bit addresses
B. I/O devices are accessed during IN and OUT instructions
C. There can be a maximum of 256 input and 256output devices
D. Logic operations can't be performed

Ans. A

Sol. Memory mapped I/O is also called as Port mapped I/O. In this technique, the same address space is shared between memory and input-output devices. For memory mapped I/O 16 Bit device address is considered.

19. One application of a digital multiplexer is to facilitate:

A. Code conversion
B. Parity checking
C. Parallel-to-serial data conversion
D. Data generation

Ans. C

Sol. Digital multiplexer consists of selector pins that have digital values. Multiplexer means many to one. In a multiplexer, many parallel data streams are sent as input, and output is obtained by selecting a particular input line. So, it is a parallel to serial converter.

20. To multiply a number by 8 in 8085 we have to use RAL instruction:

A. Once
B. Twice
C. Thrice
D. Four times

Ans. C

Sol. RAL is rotate accumulator left. Basically RAL operation is equivalent to multiplying by 2 every time. So when RAL instruction is executed, the accumulator is left shifted by one bit, and the value is added to itself for one time. So, basically we can write: $N= 2^n$, where 'N' is the number that is to be multiplied. So, here $2^3=8$. Answer is option (c)

21. The output of an exclusive–NOR gate is 1. Which input combination is correct?

A. A = 1, B = 0
B. A = 0, B = 1
C. A = 0, B = 0
D. None of these

Ans. C

Sol. The exclusive- NOR gate is the logical complement of the exclusive-OR gate. With logical inputs A and B, the output of the XNOR gate is obtained as:

$$Y = A \cdot B + \overline{A} \cdot \overline{B}$$

Hence, the output of the XNOR gate is 1, when both the inputs A and B are same. Thus, the output is 1, when A = 0, and B = 0.

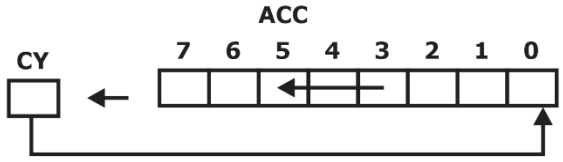
22. Initially the number decimal 8 is stored. If instruction RAL is executed twice, the final number stored will be:

A. Decimals 8 B. Decimal 16

C. Decimal 32 D. Decimal 2

Ans. C

Sol. When the RAL instruction is executed, the contents of the accumulator are shifted left one position through the carry(CY) flag, as shown below.



The least significant bit is set equal to the carry flag and the carry flag is set equal to the most significant bit.

Now, given that the decimal number 8 is stored in the accumulator. Hence, the accumulator contents are 00001000 and 0 is stored in the CY flag.

When RAL instruction is executed once, the accumulator contents are shifted left through carry, and hence becomes 00010000 (decimal 16) and 0 is stored in the CY flag.

When RAL instruction is executed again, the accumulator contents are again shifted left through carry, and hence becomes 00100000 (decimal 32) and 0 is stored in the CY flag.

23. The output of an AND gate with three inputs, A, B, andC, is HIGH when _____:

A. A = 1, B = 1, C = 0 B. A = 0, B = 0, C = 0

C. A = 1, B = 1, C = 1 D. A = 1, B = 0, C = 1

Ans. C

Sol. For three inputs A, B and C, the output of the AND gate is obtained as:

Y = A . B. C

The AND gate output is HIGH (1), when all the inputs equal to 1,

i.e., A = 1, B = 1 and C = 1.

24. A NOR gate is equivalent to a bubbled AND gate. This statement is an outcome of:

A. De Morgan's Law B. Involution Law

C. Law of Absorption D. Idempotent Law

Ans. A

Sol. For two logical inputs A and B, the NOR gate is equivalent to a bubbled AND gate. Hence,

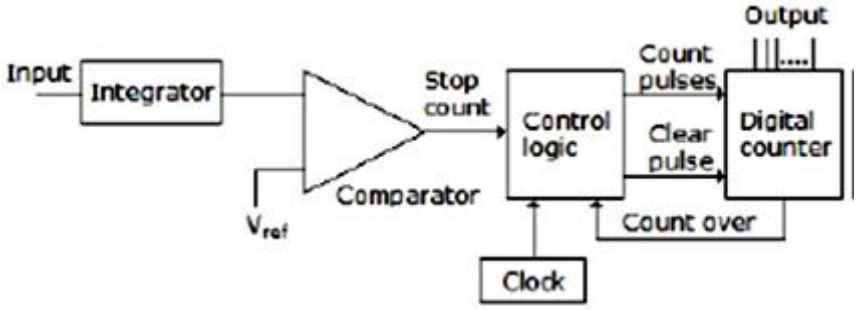
$\overline{A \cdot B} = \overline{A} + \overline{B}$

This relation is referred as the DeMorgan's theorem.

According to the DeMorgan's theorem, for any two digital signals A and B, two relations are stated,

$\overline{A + B} = \overline{A} \cdot \overline{B}$ and $\overline{A \cdot B} = \overline{A} + \overline{B}$

25. This figure is a block diagram of _____:



A. ADC
B. DAC
C. Comparator
D. 555 timer

Ans. A

Sol. The given block diagram is that of a dual-slope ADC. Analog to digital converter is the system that converts an analog signal to a digital signal.

The analog signal to be converted is applied to the integrator, and the digital output is obtained from the counter operating in the positive and negative slopes of the integrator. For a fixed time interval, the input analog signal increases the voltage at the comparator input. After the fixed time interval, the integrator output decreases at a fixed rate. During this time, the counter advances its count. As the integrator output drops below the comparator reference voltage, a signal is sent to the control logic to stop the count. The value stored in the counter is the digital output of the ADC.

26. Which of the following relation is true for two digital signals A and B?

A. $\overline{A + B} = \overline{A} \cdot \overline{B}$
B. $\overline{A + B} = A \cdot B$
C. $\overline{A + B} = \overline{A} \cdot \overline{B} + A \cdot B$
D. $\overline{A + B} = \overline{A} \cdot B$

Ans. A

Sol. According to the DeMorgan's theorem, for any two digital signals A and B, we have,

$\overline{A + B} = \overline{A} \cdot \overline{B}$ and $\overline{A \cdot B} = \overline{A} + \overline{B}$

27. An eight bit digital data 10101100 is fed to an ADC. The reference voltage is +10V. The analog output voltage will be:

A. 1.05V B. 6.74V

C. 10.10V D. 5.15V

Ans. B

Sol. Here given n=8, and input data is 10101100(172 in decimal).

So, output voltage V_{out} = [Ref. Voltage/ (2^n-1)] * 172 ⇒ (1720/ 255) ⇒ 6.74 V

28. 11001, 1001 and 111001 corresponding to the 2's complement representation of which one of the following sets of number?

A. 25, 9 and 57 respectively B. –6, –6 and –6 respectively

C. –7, –7 and –7 respectively D. –25, –9 and –57 respectively

Ans. C

Sol. Check for 1st number: 11001 ⇒ 1's complement ⇒ 00110 +1 ⇒ 2's complement ⇒ 00111(7 in decimal)

Check for 2nd number: 1001 ⇒ 1's complement ⇒ 0110 + 1 ⇒ 2's complement ⇒ 0111(7 in decimal)

Since both are 7, therefore, the only option that matches the first two is option (c). So, it is the correct answer.

29. The Boolean expression for the truth table shown is:

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

A. $B(A+C)(\bar{A}+\bar{C})$ B. $B(A+\bar{C})(\bar{A}+C)$

C. $\bar{B}(A+\bar{C})(\bar{A}+C)$ D. $\bar{B}(A+C)(\bar{A}+\bar{C})$

Ans. A

Sol. We observe that the expression needed in the result is of POS form but in a truth table, the output is 0 for many terms but 1 only for 2 terms so we write the SOP equation. Then convert it to POS.

F = A' BC + ABC'

$\Rightarrow$ B (A' C + AC')

$\Rightarrow$ B (A $\oplus$ C)

$\Rightarrow$ B (A + C) (A' + C')

Since

$A \oplus C = A \odot C = AC + \overline{A}\,\overline{C}$

So, $\overline{A \odot C} = \overline{AC + \overline{A}\,\overline{C}}$

$= \left(\overline{A} + \overline{C}\right)\left(A + C\right)$

$\left(A \oplus C\right)$

30. Which of the following is used as a data selector?

A. Encoder B. Decoder

C. Multiplexer D. De-multiplexer

Ans. C

Sol. Multiplexer in general has 2^n inputs and one output line. Multiplexer means "many into one". It means it is a device which selects a particular analog input line by the help of select line, and forwards that selected line towards the output line. This is why it is called as data selector.

31. A phase-locked loop (PLL) is a feedback circuit consisting of a:

A. Phase detector B. Low-pass filter

C. VCO D. All of these

Ans. D

Sol. A phase locked loop is an electronic circuit whose output remains in phase with the input signal. PLL consists of a phase detector, LPF, VCO and an Error amplifier. The phase detector compares input and feedback frequency, the LPF removes high frequency noise, VCO(voltage controlled oscillator) is used to adjust the feedback frequency according to the input signal frequency. Also, the error amplifier amplifies the error signal.

32. In a microprocessor:

A. One machine cycle is equal to one clock cycle

B. One clock cycle consists of several machine cycles

C. One machine cycle consists of several clock cycles

D. One machine cycle is always less than one clock cycle

Ans. C

Sol. Machine cycle is also called as instruction cycle. Generally instruction cycle= Fetch cycle+ Execution cycle. In fetch cycle opcode is fetched from memory, and in execution cycle, either read or write operation is performed. Machine cycle consists of several clock cycles.

33. The fast carry or look-ahead carry circuits found in most 4-bit parallel-adder circuits:

A. Increase ripple delay
B. Add a 1 to complemented inputs
C. Reduce propagation delay
D. Determine sign and magnitude

Ans. C

Sol. Carry look ahead adder circuits generally reduces delay by increasing speed of operation. It does this by reducing the time required for carry calculation in each stage.

34. A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 1010:

A. 0.3125 V
B. 3.125 V
C. 0.78125 V
D. –3.125 V

Ans. B

Sol. Given,
4bit R/2R DAC. V_{ref} = 5 volts, and input code= 1010. We have to find ⇒ V_{out}
Now, For R-2R Ladder, formula can be given as:
Vout = Vref/2^n (msb bit*2^0 + next bit*2^1 + next bit*2^2 + lsb bit*2^3)
= 5/16(0 + 2 + 0 + 8) ⇒ 3.125V

35. PLAs, CPLDs, and FPGAs are all which type of device?

A. SLD
B. PLD
C. EPROM
D. SRAM

Ans. B

Sol. Programmable Logic devices(PLDs) are electronics components that are basically used to make reprogrammable digital circuits. Its function remains un-defined during the time of manufacturing, and it contains array of AND and OR gates.

36. A blank EPROM has:

A. All bits set to logical 0
B. All bits set to logical 1
C. Half the total number of bits set to 0 and remaining half to logical 1
D. Either A. or B.

Ans. B

Sol. EPROM is erasable programmable read only memory. It is a chip(ROM Type) that can hold data for many years. The cells of EPROM consists of transistors, and has an array of rows and columns. The cells of a blank EPROM has a value of 1.

37. The output waveform of a 555 Timer is:

A. Sinusoidal
B. Triangular
C. Rectangular
D. Elliptical

Ans. C

Sol. A 555 timer produces a rectangular output. It operates in two modes: mono-stable and astable.

When operating in the mono-stable mode, a trigger is applied to it and the output switches from low to high and after a time delay returns back to the low state, and remains low until another trigger arrives, thereby producing a rectangular output.

In astable mode, it does not require any trigger. It has no stable state and hence does not remain indefinitely in either state. It oscillates between the low and high state and produces a rectangular output.

38. Another name for a digital multiplexer is

A. data selector
B. compressor
C. Encoder
D. Decoder

Ans. A

Sol. A multiplexer connects one the input to the output according to the data on select lines so it is called as data selector.

39. A multiplexer is described by its size through , where n = number of bits.

A. $n \times 2^n$
B. 1×2^n
C. $2^n \times 1$
D. $2^n \times n$

Ans. C

Sol. A multiplexer is described by its size through $2^n \times 1$, where n = number of bits.

40. In which gate you must have two or more low inputs to get the low output

A. AND
B. Inverter
C. OR
D. NAND

Ans. C

Sol. Two get low output for an OR gate, all the inputs must be low.

41. A solid state device which only gives "1" output if all inputs are also "1" is called

A. AND gate
B. OR gate
C. NAND gate
D. NOR gate

Ans. A

Sol. In case of AND gate output is product of all the inputs applied. So as to get "1" as output you must apply all input "1".

42. Which two input gate produces logic "1" output if both the inputs are different and otherwise produces logic "0" output.

A. AND
B. OR
C. XOR
D. XNOR

Ans. C

Sol.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$\therefore\ Y = A \oplus B$

43. Which of the following are the universal gates

A. OR and NAND
B. AND and NAND
C. OR and NOR
D. NOR and NAND

Ans. D

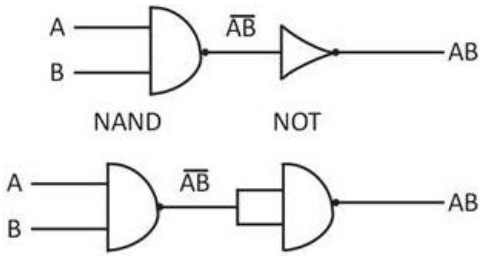
Sol. All gates can be derived either using NOR gates or using NAND gates so they are universal gates.

44. How many NAND gates are required to implement AND gate?

A. 2
B. 3
C. 4
D. 5

Ans. A

Sol.



45. _____ is a single bit comparator

A. wired OR
B. exclusive OR
C. NOR
D. exclusive NOR

Ans. D

Sol. Exclusive NOR gate produces output "1" when both the inputs are same so it can be used as single bit comparator.

46. How many flip-flops are required for counter that will count 0 to 255?

A. 2
B. 4
C. 16
D. 8

Ans. D

Sol. Since the counter is counting from 0 to 255 i.e. 256 states 8 flip-flops must be required as $2^8 = 256$.

47. A counter circuit is usually constructed of _____.

A. A number of latches connected in cascade form
B. A number of NAND gates connected in cascade form

C. A number of flip-flops connected in cascade

D. A number of NOR gates connected in cascade form

Ans. C

Sol. A counter circuit is usually constructed of a number of flip-flops connected in cascade. Preferably, JK Flip-flops are used to construct counters and registers.

48. The duty cycle of the most significant bit (MSB) from a 4-bit BCD counter is _____.

A. 20% B. 50%

C. 10% D. 80%

Ans. A

Sol. There are 10 states, out of which MSB is high only for (1000, 1001) 2 times. Hence duty cycle is 2/10*100 = 20%. Since the duty cycle is the ratio of on-time to the total time.

49. Which counters are often used whenever pulses are to be counted and the results displayed in decimal?

A. Synchronous B. Bean

C. Decade D. BCD

Ans. D

Sol. BCD means Binary Coded Decimal, which means that decimal numbers coded of binary numbers. It displays the decimal equivalent of corresponding binary numbers.

50. UP-DOWN counter is also known as _____.

A. Dual counter B. Multi counter

C. Multimode counter D. Two Counter

Ans. C

Sol. UP-DOWN counter is also known as multimode counter because it has capability of counting upward as well as downwards.

51. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?

A. Parallel-in Parallel-out B. Parallel-in Serial-out

C. Serial-in Serial-out D. Serial-in Parallel-out

Ans. C

Sol. Serial-in Serial-out register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time. Since in serial transmission, bits are transmitted or received one at a time and not simultaneously.

52. From a 3-bit binary counter design using T flip- flops, determine the number of T flip-flops needed in its circuit implementation.

A. 1 B. 2

C. 3 D. 4

Ans. C

Sol. For a n-bit counter we always require N number of flip-flops so From a 3-bit binary counter design using T flip- flops 3 T flip-flops needed in its circuit implementation.

53. A binary counter that counts from 0000 to 1001 before it recycles.

A. buffer B. BCD counter

C. ring counter D. ripple counter

Ans. B

Sol. The given counter counts from 0000 to 1001 before it recycles that means it has 10 stable states so it is called BCD counter.

54. It is the required interval immediately following the active edge held of clocks during which the control inputs must be held.

A. set-up time B. hold time

C. pulsing time D. propagation time

Ans. B

Sol. Hold time is the required interval immediately following the active edge held of clocks during which the control inputs must be held.

55. A JK flip-flop can be made to function like a T flip-flop by simply

A. connecting the J and K inputs together as one-input

B. connecting J = 0 and K = 0

C. resetting all inputs of the JK

D. connecting earth ground the JK inputs

Ans. A

Sol. If you short the J and K terminals of JK flip-flop it becomes T flip-flop.
Because if you give J = 0 and K = 0 present state remains as it is and if you give J = 1 and K = 1 present state gets toggled.

56. If you connect a not gate between J and K terminals of JK flip-flop it becomes flip-flop.

A. D B. T

C. S-R D. C

Ans. A

Sol. If you short connect a not gate between J and K terminals of JK flip-flop it becomes D flip-flop.
Because if you give J = 0 and K= 1 next state will be 0 and if you give J = 1 and K= 0 next state will be 1.

57. The state of the flip-flop after the occurrence of a clock pulse is called as its

A. current state B. present state

C. next state D. current input

Ans. C

Sol. The state of the flip-flop before the occurrence of clock pulse is called as its next state.

58. _____ refers to BCD counter

A. Decade counter B. frequency divider

C. shift register D. Binary counter

Ans. A

Sol. A BCD counter has only 10 valid states. So it can also be termed as a decode counter.

59. The state of the flip-flop before the occurrence of clock pulse is called as its

A. present state B. next state

C. current input D. present output

Ans. A

Sol. The state of the flip-flop before the occurrence of clock pulse is called as its present state.

60. _____ is not a type of flip-flop?

A. RS Flip Flop B. JK Flip flop

C. D Flip Flop D. Register

Ans. D

Sol. Registers are used to store the data but as they are not clock operated they are not flip-flop.

61. In positive edge triggering the change of state occurs when

A. The pulse level is high

B. The pulse level is low

C. The pulse level is going from low to high

D. The pulse level is going from high to low

Ans. C

Sol. In a positive edge triggered flipflop, the flipflop, the flip flop is triggered when the pulse level is going from low to high.

62. A flipflop whose output is always the same as its input?

A. RS flipflop B. D flipflop

C. T flipflop D. JK flipflop

Ans. B

Sol. In D flipflop output is always same as input, that's why it can be used as a delay element.

63. A RS flip-flop constructed from NOR gates would have an undefined output when the inputs RS combinations are

A. Low/Low B. Low/High

C. High/Low D. High/High

Ans. D

Sol. When both R and S becomes high both Q_n and $\overline{Q_n}$ becomes zero which is not possible so it is called undefined output.

64. Combination of flip-flop, arranged so that they can be triggered at the same time

A. clocked synchronous flip-flop B. Delayed flip-flop

C. sequential flip-flop D. Asynchronous flip-flop

Ans. A

Sol. As the flipflops are triggered at the same time they are synchronous clocked flip-flops

65. Read following

i. sequential circuit uses flip flops

ii. sequential circuit uses clock

iii. sequential circuit has less hardware requirement compared to combinational

iv. sequential circuit output depends on input only

A. All are true B. i and ii

C. i and iii D. i, ii, iv

Ans. B

Sol. Sequential circuit has flip flops uses clocks and more hardware required as compared to combinational output depends on previous state and present input.

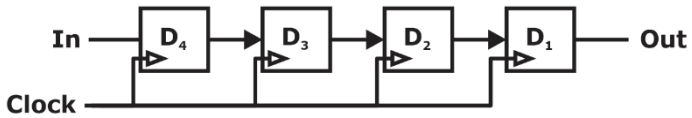
66. For a serial in serial out register of 4 bits time taken for output of 4 bits is

A. 4 B. 5

C. 3 D. 1

Ans. C

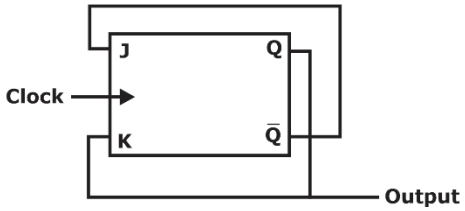
Sol.



For serial In serial Out the date to be seen at output (n-1) clock pulse will be needed where n is number of bits. 4 bits are there so (4-1)=3 clock pulse will be needed to obtain In at Out.

At 3rd clock pulse data at In will be shown at Out.

67. Given below is a circuit using JK flip flop and is initially reset, after 5 clock pulse find the sequence at output 'Q'.

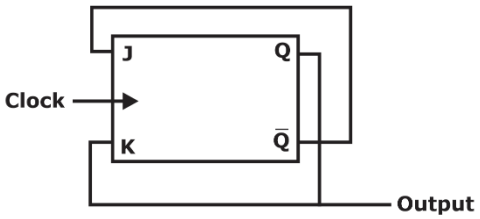


A. 10101 B. 010101

C. 011001 D. 111111

Ans. A

Sol.



It is biased as frequency divider and will be in toggle mode.

at

Clock	States
X	0
1	1
2	0
3	1
4	0
5	1

68. The expression Y = A.1 will be equivalent to

A. A B. 1

C. 0 D. can't be determined

Ans. A

Sol. (.) is AND operator

Truth table for AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

If B = 1, Y = A

For B.A = A.1 = A

69. The Universal gates are

A. NAND B. NOR

C. AND D. OR

Ans. A

Sol. NAND & NOR is used to implement any gate.

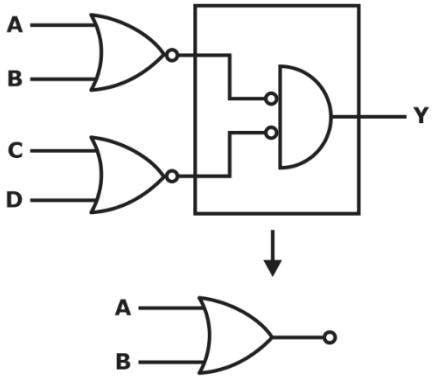
70. Number of NOR gates to implement logic Y = (A + B) (C + D) will be :

A. 4 B. 5

C. 3 D. 6

Ans. C

Sol. Y = (A + B) (C + D)



Bubbled AND = NOR gate

71. The reduced expression for given equation.

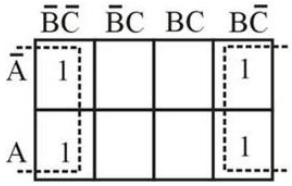
$Y = \bar{A} \times \bar{B} \times \bar{C} + \bar{A} \times B \times \bar{C} + A \times \bar{B} \times \bar{C} + A \times B \times \bar{C}$

A. $\bar{B}\bar{C} + BC$ B. $\bar{A} + \bar{C}$

C. $\bar{C}$ D. None of above

Ans. C

Sol. K-map



Quad pair is formed, so the reduced expression gives

$Y = \bar{C}$

72. If F = AB + A'B' Boolean expression is to be implemented using decoders and OR gates, the connection involves

A. 2 to 4 line decoder with 3 OR gates

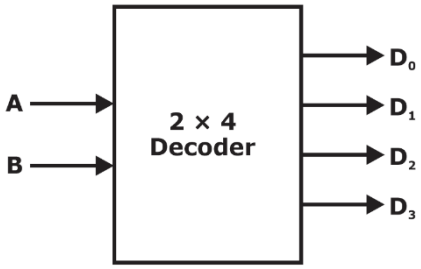
B. 3 to 8 line decoder with 2 OR gates

C. 2 to 4 line decoder with 1 OR gates

D. 3 to 8 line decoder with 4 OR gates

Ans. C

Sol. F = AB + A'B' Boolean expression is to be implemented using decoders and OR gates, the connection involves 2 to 4 line decoder with 1 OR gates



If you add D1 and D2 with OR gate you will get F = AB + A'B'.

73. Which of the following is a form of De Morgan's theorem?

A. A + B = (AB)'

B. AB = (A + B)'

C. (A + B)' = A' . B'

D. A . B = A' . B'

Ans. C

Sol. De Morgan's theorem is used to find the compliment of a function

(A + B)' = A' . B' is the only valid identity among the given options.

74. The operation result will be 1 if any one or more variables is a 1.

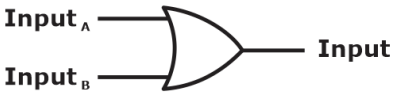
A. NOT B. AND

C. OR D. NOR

Ans. C

Sol. The operation result will be 1 if any one or more variables is a 1 is OR operation as the truth table for OR gate is

2 – input OR gate



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

75. A circuit that changes a code into a set of signals is called

A. encoder B. decoder

C. multiplexer D. data selecter

Ans. B

Sol. A circuit that changes a code into a set of signals is called decoder and it is opposite of the encoder.

76. A decoder with 4 inputs can have a maximum of how many outputs?

A. 4 B. 8

C. 16 D. 32

Ans. C

Sol. A decoder with 4 inputs can have a maximum of 16 outputs as $2^4 = 16$.

77. A command to an ADC to start conversion.

A. SOC B. EOC

C. PAC D. EAR

Ans. A

Sol. SOC i.e. Start of Conversion is used in ADC to start conversion and EOC i.e. End of Conversion is used to indicate that conversion has completed.

78. In integrating type ADCs, the

A. Input voltage is proportional to input averaged over the integration period

B. Output voltage is proportional to sum of input voltage

C. Output voltage is proportional to input averaged over the integration period

D. Input voltage is proportional to sum of input voltage

Ans. C

Sol. Since the integrating type ADC do not require sample and hold circuit at the input. The change in input during conversion will not affect the output code and is proportional to the value of the input averaged over the integration period.

79. Express the output voltage of digital to analog converter?

A. $V_o = KV_{FS}(d_1 2^{-1} + d_2 2^{-2} + \ldots. d_n 2^{-n})$ B. $V_o = V_{FS}/k(d_1 2\text{-}1 + d_2 2^{-2} + \ldots. d_n 2^{-n})$

C. $V_o = V_{FS}(d_1 2\text{-}1 + d_2 2^{-2} + \ldots. d_n 2^{-n})$ D. $V_o = K(d_1 2\text{-}1 + d_2 2^{-2} + \ldots. d_n 2^{-n})$

Ans. A

Sol. The input is an n-bit binary word D and is combined with the reference voltage V_R to give on analog output signal. Mathematically it is described as $V_o = KV_{FS}(d_1 2^{-1} + d_2 2^{-2} + \ldots. d_n 2^{-n})$ where, K-scaling factor, V_{FS}-full scale output voltage.

80. The smallest resistor in an 8 bit weighted resistor DAC is 5kΩ, what will be the largest resistor value?

A. 2.56MΩ B. 1.28MΩ

C. 1.28KΩ D. 2.56KΩ

Ans. B

Sol. The largest resistor value for 8-bit DAC= $2^n \times R = 2^8 \times 5k\Omega = 256 \times 5k\Omega = 1.28M\Omega$

81. How to overcome the limitation of binary weighted resistor type DAC?

A. Using hybrid DAC B. Multiplying DACs

C. Using monolithic DAC D. Using R-2R ladder type DAC

Ans. D

Sol. Usage wide range of resistors is the limitation of binary weighted resistor type DAC, this can be avoided by using R-2R ladder type DAC Where only two value of resistor are required.

82. Which of the items below can perform parallel- to-serial data conversion?

A. shift register
B. binary counter
C. multiplexer
D. decoder

Ans. A

Sol. A shift register can perform parallel- to-serial data conversion. The series of shift registers connected in PISO mode are used for parallel- to-serial data conversion.

83. Which of the following does not form DAC's?

A. counter
B. resistor network
C. current switches
D. reference

Ans. A

Sol. Counters are not used in DAC's rather they are used in ADC's. Resistor network, current switches, reference voltage source are used in DAC's.

84. What does a computer do with the data it receives from an ADC?

A. stores the data
B. performs calculation
C. processes the data
D. all of the choices

Ans. D

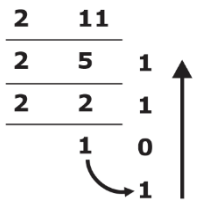
Sol. When a computer receives data from an ADC it stores the data, performs calculation and processes the data.

85. Find equivalent decimal number of 11?

A. 1101
B. 1110
C. 1111
D. 1011

Ans. D

Sol.



$\therefore (11)_{10} = (1011)_2$

86. Which of the following is not used in hexadecimal digital symbols?

A. A
B. C
C. H
D. F

Ans. C

Sol. In hexadecimal system letters up to F only are used.

87. Find the sum of $(110.1101)_2$ and $(11.01)_2$

A. 1010.0101
B. 1101.0101
C. 1010.0001
D. 0111.1010

Ans. C

Sol.

$$\begin{array}{r} 1\ 1\ 0\ .\ 1\ 1\ 0\ 1 \\ +\quad 1\ 1\ .\ 0\ 1 \\ \hline 1\ 0\ 1\ 0\ .\ 0\ 0\ 0\ 1 \end{array}$$

$\therefore (1010 . 0001)_2$

88. Find 2's compliment of (1101.1100)2

A. 0010.0011 B. 10.01

C. 10.0011 D. 0010.0100

Ans. D

Sol. 2's compliment is 1's compliment + 1

$$\begin{array}{r} 1\ 1\ 1\ 1\ .\ 1\ 1\ 1\ 1 \\ -1\ 1\ 0\ 1\ .\ 1\ 1\ 0\ 0 \\ \hline 0\ 0\ 1\ 0\ .\ 0\ 0\ 1\ 1 \\ +1 \\ \hline 0\ 0\ 1\ 0\ .\ 0\ 1\ 0\ 0 \end{array}$$

89. The following operation leads to

$(37)_H + (29)_H = (\ )_H$

A. 60 B. 66

C. 56 D. 50

Ans. A

Sol.

$$\begin{array}{r} (37)_H \\ +(29)_H \\ \hline (60)_H \end{array}$$

90. A magnitude comparator has 2^{2n} entries in the truth table where n

A. number of inputs

B. number of comparator bits

C. number of outputs

D. number of inputs and outputs

Ans. B

Sol. If a magnitude comparator has 'n' number of comparator bits then it has 2^{2n} entries in the truth table.

91. Binary 101010 is equivalent to decimal number

A. 24 B. 42

C. 64 D. 44

Ans. B

Sol. $\rightarrow 101010)_2 = [1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^o] = [42]_{10}$

92. Which of the following logic has highest fan out

A. CMOS B. HTL

C. I^2L D. ECL

Ans. A

Sol. CMOS has least input driving current hence maximum fan out,

As gate has oxide layer so, no current goes into gate hence more devices can be driven.

93. Speed of a logic circuit is normally expressed as

A. logic levels B. noise margin

C. power consumption D. propagation delay

Ans. D

Sol. The time required for an input to reach the output is considered as the propagation delay and this propagation delay decides the speed of the devices.

94. Which of the following output configuration is available in TTL gate?

1. Open collector output
2. Totem-pole output
3. Tristate output

A. 1 only B. 1 and 2 only

C. 2 and 3 only D. 1, 2 and 3

Ans. D

Sol. All above listed are the possible output configurations in TTL gate.

1. Open Collector Output:

The main feature is that its output is 0 when low and floating when high. Usually an external Vcc may be applied.

2. Totem Pole Output:

Totem Pole means addition of an active pull up circuit in the output of the Gate which results in reduction of propagation delay

3. Tri state Gate:

It provides 3 state output.

1. Low level state when lower transistor is ON and upper transistor is OFF.
2. High level state when lower transistor is OFF and upper transistor is ON.
3. Third state when both transistors are OFF. It allows direct wire comnection of many outputs.

95. A flip flop is

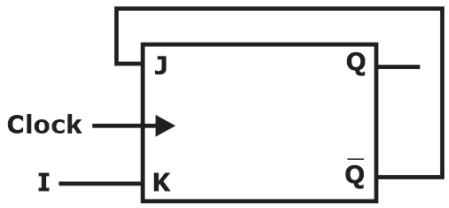
A. Monostable B. Bistable

C. Metastable D. Astable

Ans. B

Sol. Flip flop has output 1 & 0 hence it is bistable

96. The sequence generated by the following sequential circuit is

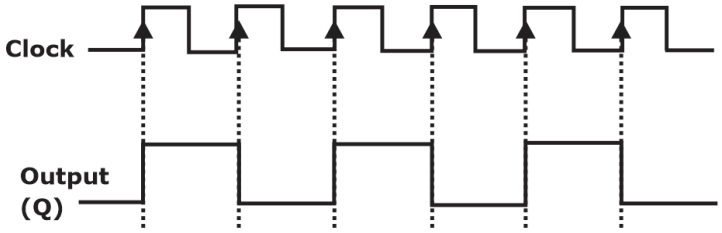


A. 010101 B. 011010

C. 10110 D. None

Ans. A

Sol. It is a frequency divider circuit and responds to positive clock edge.



97. An n-bit binary parallel adder requires _____ in its least design.

A. n half adders B. n half subtractor

C. n full adders D. n half subtractors and n full adder

Ans. C

Sol. An n-bit binary parallel adder requires n full adders in its least design or it will require (n-1) full adders and 1 half adders.

98. A block added to the combinational logic circuit to form a sequential logic circuit is the

A. ROM B. counter

C. clock D. memory

Ans. D

Sol. The only difference between a combinational logic circuit and a sequential logic circuit is the memory so if you add memory to combinational logic it becomes sequential logic circuit.

99. If you short the J and K terminals of JK flip-flop it becomes flip-flop.

A. D B. T

C. S-R D. C

Ans. B

Sol. If you short the J and K terminals of JK flip-flop it becomes T flip-flop.

Because if you give J = 0 and K= 0 present state remains as it is and if you give J = 1 and K= 1 present state gets toggled.

100. Which of the following does not describe a flip-flop?

A. it is a one-bit memory device

B. its internal circuitry is usually symmetrical

C. it is a bistable device

D. it is equivalent to a one- short circuit

Ans. D

Sol. A flip-flop is a one-bit memory device, its internal circuitry is usually symmetrical and it is a bistable device as it has two stable states 0 and 1.

****