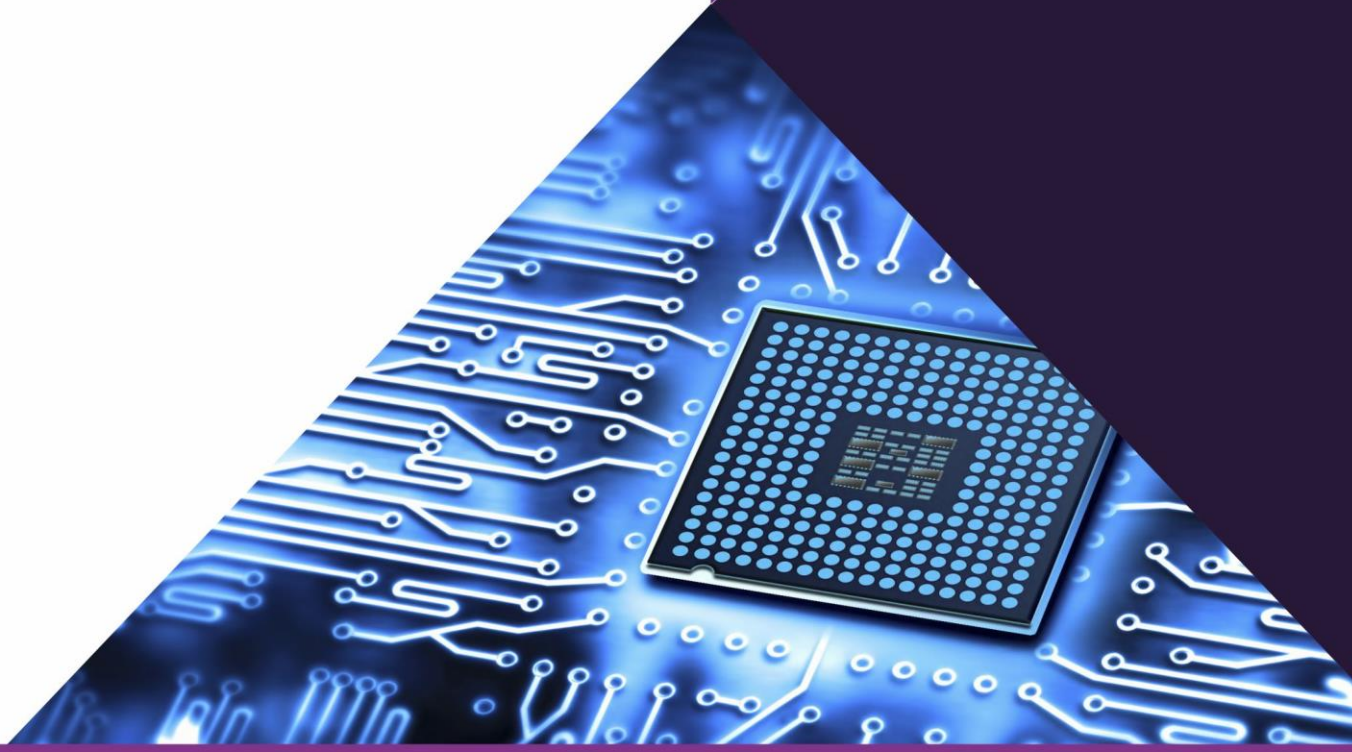
BYJU'S EXAM PREP

Electronics Engineering

Analog Circuits

SHORT NOTES



IMPORTANT FORMULAS TO REMEMBER

CHAPTER 1: DIODE CIRCUITS

1.Diode models:

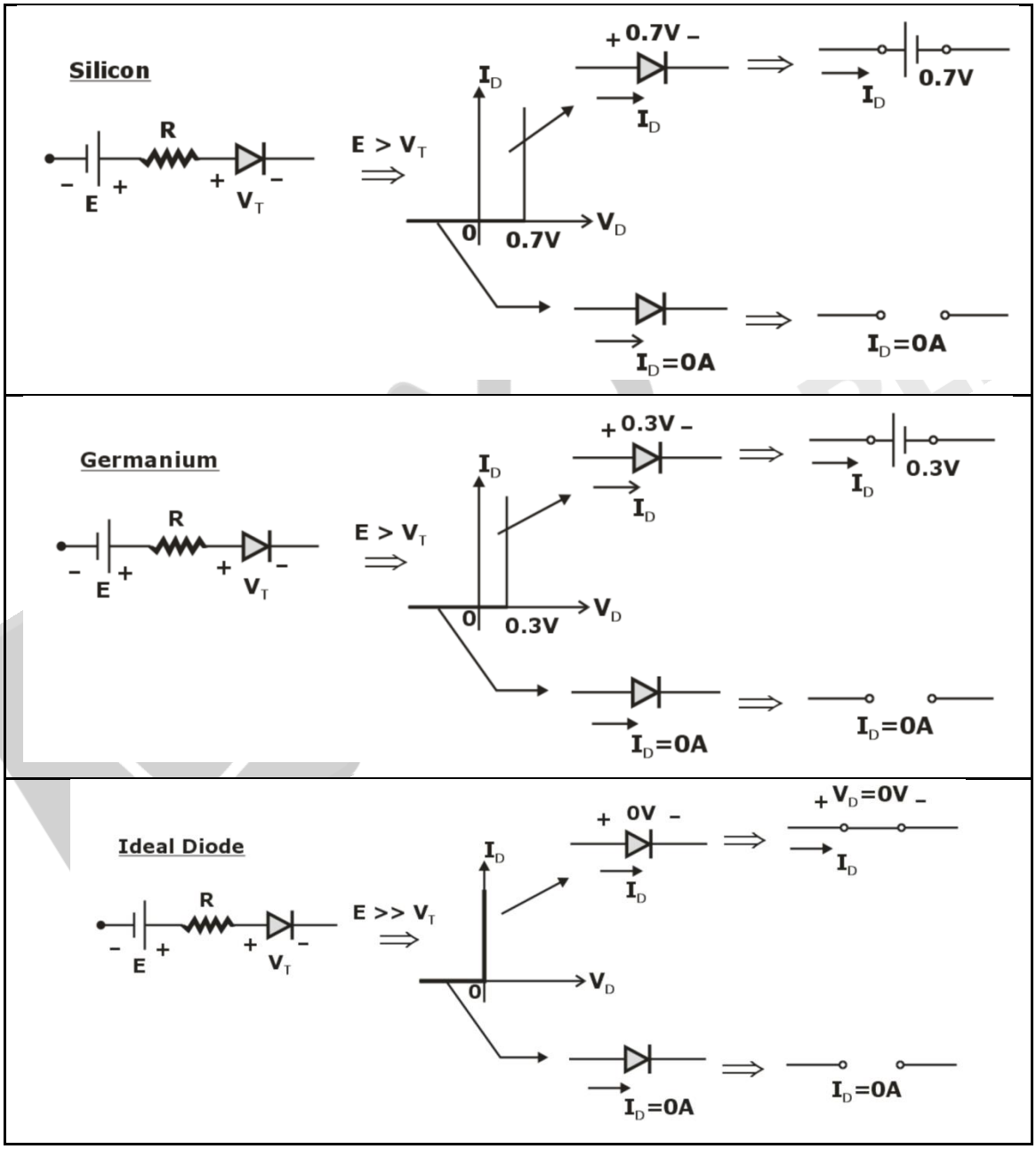


Figure 1: Approximate and ideal semiconductor diode models.

2. V-I Characteristics:

A diode is an active unidirectional of non-linear device.

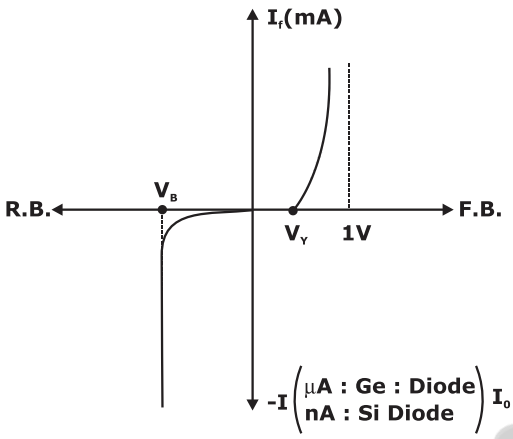
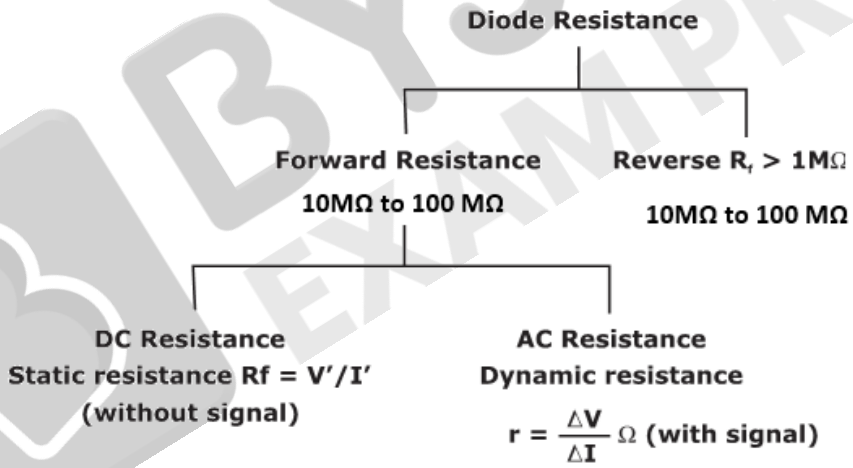


Figure 2: V-I characteristics

Breakdown voltage of diode is the manufactures specification. So, in any type of PN-junction.

$$V_{Br.} \alpha \frac{1}{\text{Doping}}$$

3.Diode Resistance:



3.1.Dynamic Resistance of Diode:

$$r = \frac{dV}{dI}; r = \frac{\eta V_T}{I}$$

$I >> I_0$ for a forward current I = 26 mA

$r_{si} > r_{Ge}$

Diode small signal conductance:

$$g = \frac{I_D}{\eta V_T}$$

4.Temperature Dependence of V-I Characteristics:

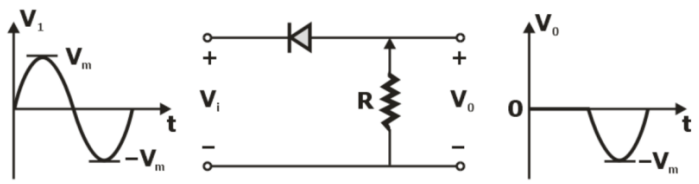
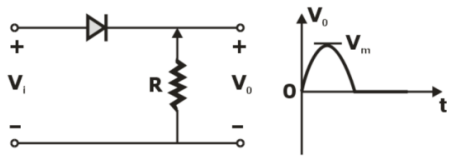
1.Reverse saturation current approximately doubles for every 10°C rise in temperature

$$I_{02}(T) = I_{01} \times 2^{(T2-T1)/10}$$

2.For either silicon or Ge at room temperature,

$$\frac{dV}{dT} = -2.5\,mV/^{\circ}C$$

5.Summary of series & parallel clipper :

Positive	Negative
Simple series clippers (Ideal diode) 	

Based series Clippers (Ideal Diodes)

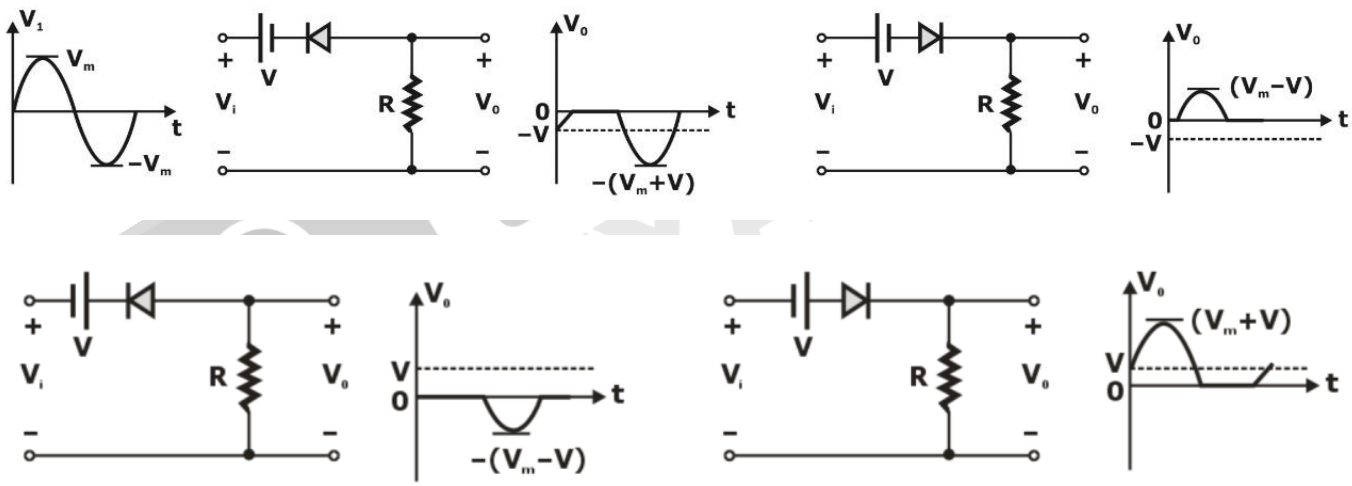
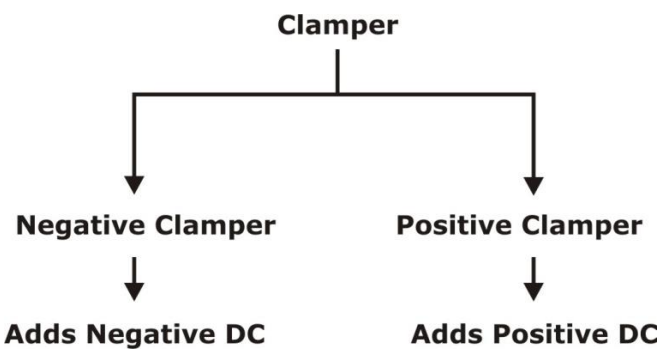


Figure 3

6.CLAMPER



6.1. Negative clamper

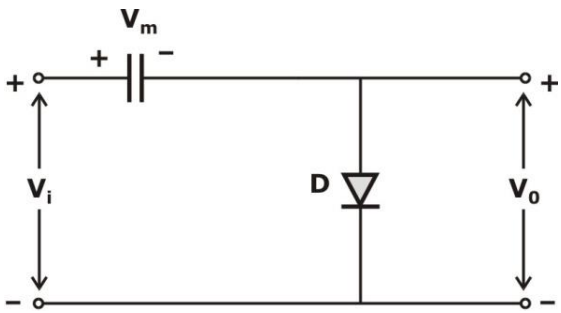


Fig 4(a): Ideal clamper circuit

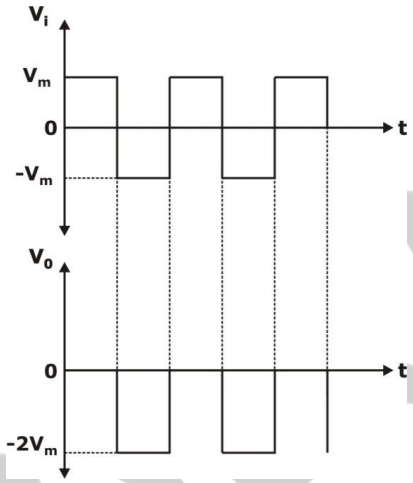


Fig 4(b): waveform

6.2. Negative clamper with voltage source:

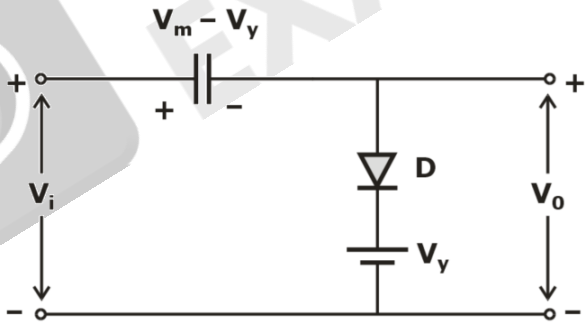


Figure 5(a)

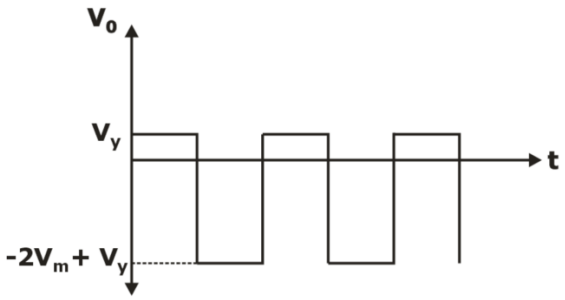


Figure 5(b): Waveform

6.2. Positive clamper :

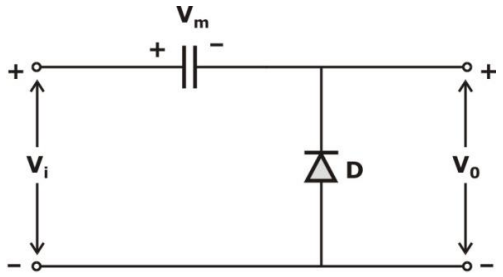


Figure 6(a): Positive clamper circuit

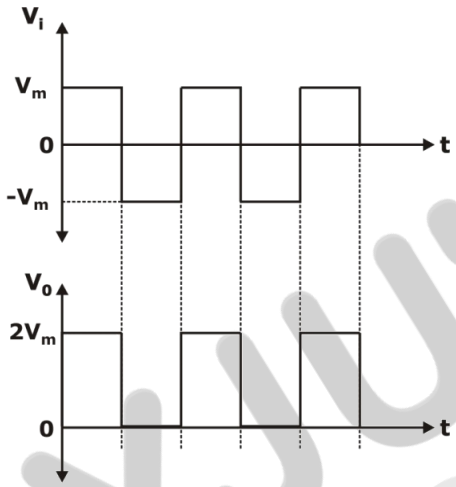


Figure 6(b): Waveform

7.VOLTAGE MULTIPLIER :

7.1. Voltage doubler:

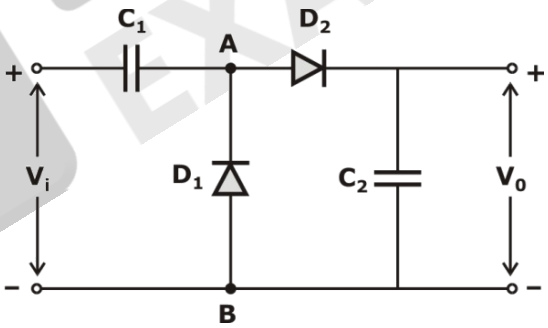


Figure 7(a): Voltage doubler circuit

$V_{AB} = V_m + V_m = 2V_m$

7.2. Voltage tripler/Quadrupler :

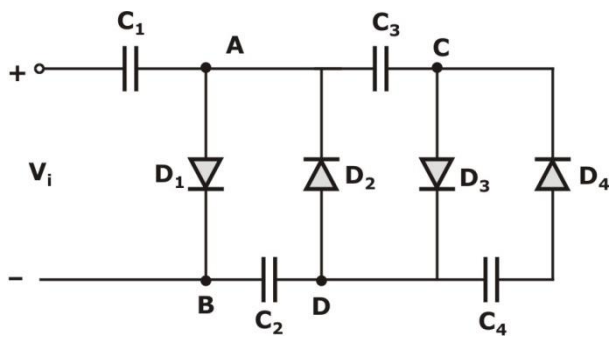
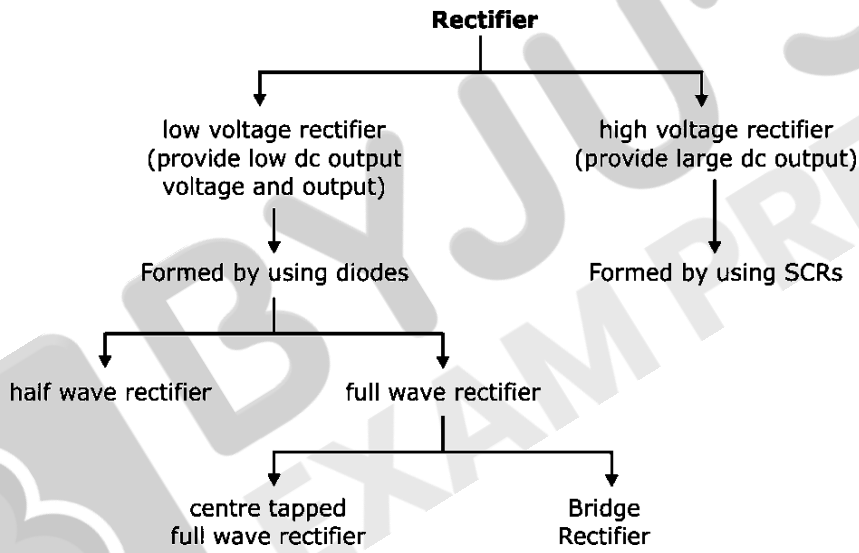


Figure 7(b): Voltage tripler/Quadrupler circuit

8. DIODE AS RECTIFIER:



8.1. Half wave Rectifier

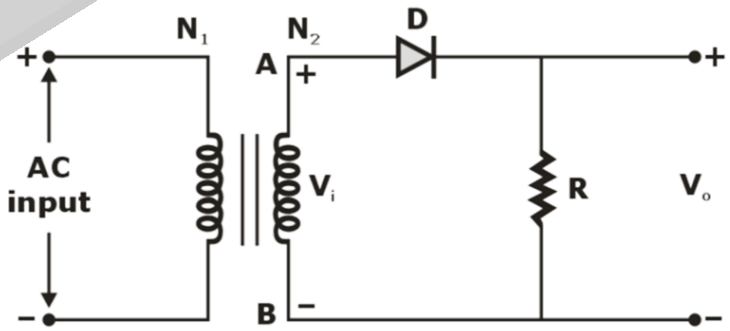


Figure 8(a): Half Wave Rectifier

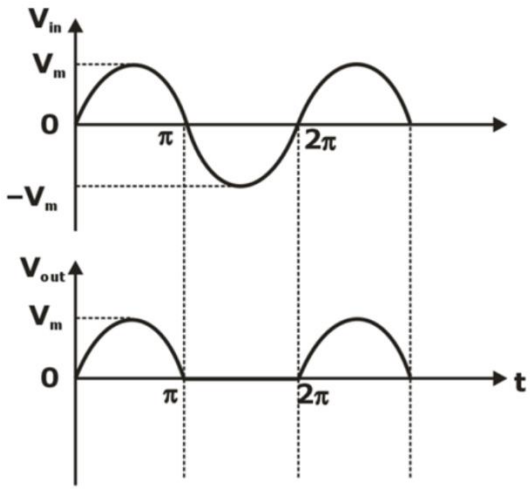


Figure 8 (b): Input and Output waveform

a. $V_o(DC) = \frac{V_m}{\pi}$

b. $I_o(DC) = \frac{V_o(DC)}{R} = \frac{V_m}{R\pi} = \frac{I_m}{\pi}$

c. $V_o(rms) = \frac{V_m}{2}$

d. $I_o(rms) = \frac{I_m}{2}$

e. $\gamma = \sqrt{\left(\frac{V_o(rms)}{V_o(DC)}\right)^2 - 1} = \sqrt{\left[\frac{I_o(rms)}{I_o(DC)}\right]^2 - 1}$

f. $\gamma = 1.21$ ➔ $\gamma(\%) = 121\%$

g. $PIV = V_m$

h. $\eta = \frac{P_o(dc)}{P_{in}(ac)} \times 100$ ➔ $\eta = 40.5\%$

i. $FF = 1.57$

j. $TUF = 28\%$

k. Peak factor $= \frac{I_m}{I_{rms}} = \frac{I_m}{I_m/2} \Rightarrow 2$

l. Time period = T = 2π , Frequency f(out) = f(in)

8.2.Disadvantage of half wave rectifier:

(i) V_o (DC) = 0.318 V_m

Output DC voltage is only 31.8% of peak input voltage V_m

(ii) η = 40.5%

Efficiency is only 40.5%, that is only 40.5% is converted into DC remaining will be lost.

9.Full Wave Rectifier:

9.1.Centre-Tapped Full-wave Rectifier:

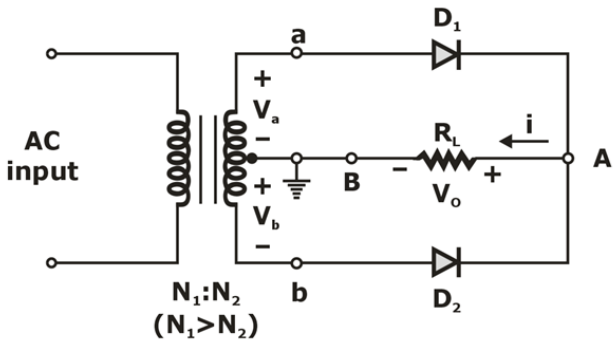
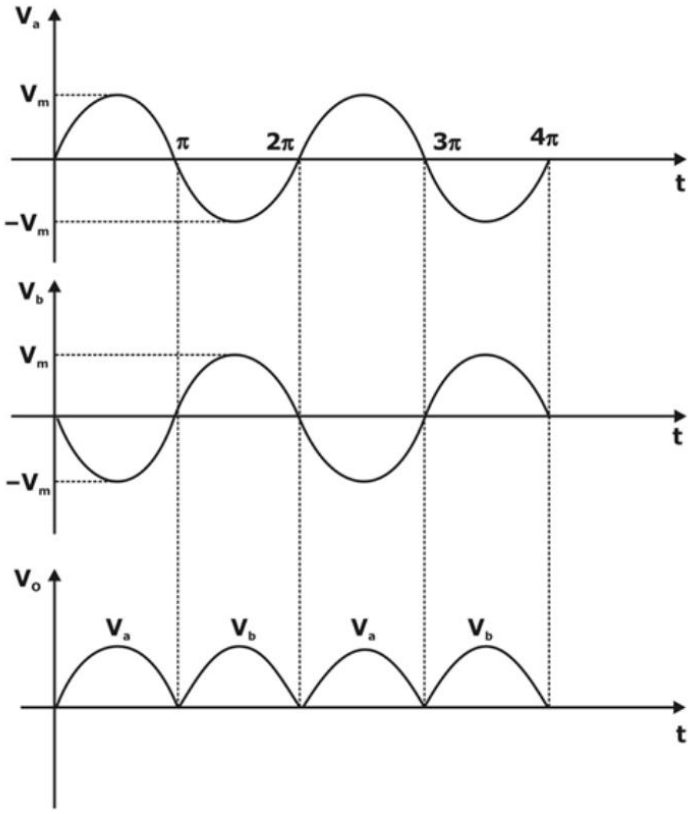


Fig 9(a)



(b)

Figure 9: (b) Centre tap rectifier circuit, (c) waveform

i. $\boxed{V_o\,(DC) = \frac{2V_m}{\pi} = 0.636V_m}$

ii. $\boxed{I_o\,(DC) = \frac{2I_m}{\pi} = 0.636\,I_m}$

iii. $\boxed{V_o\,(rms) = \frac{V_m}{\sqrt{2}}}$

iv. $\boxed{I_o\,(rms) = \frac{I_m}{\sqrt{2}}}$

v. $\boxed{\gamma = 0.483}$ ➔ $\boxed{\gamma(\%) = 48.3\%}$

vi. $\boxed{\eta = 81\%}$

vii. $\boxed{PIV = 2V_m}$

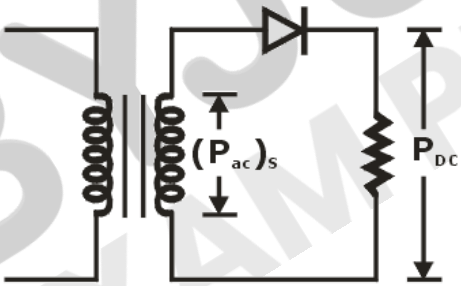


Figure 10

viii. $$TUF = \frac{TUF_{(primary)} + TUF_{(secondary)}}{2}$$

$$(TUF)_p = \frac{P_{DC}}{(P_{ac})_p} = 69\%$$

ix. $\boxed{FF = 1.11}$

x. $$\text{Peak factor} = \frac{I_m}{I_{rms}} = \frac{I_m}{I_m/\sqrt{2}} \Rightarrow \sqrt{2}$$

xi. Time period, T = T/2 = π , Frequency f(out) = 2*f(in)

9.2. Bridge Rectifier

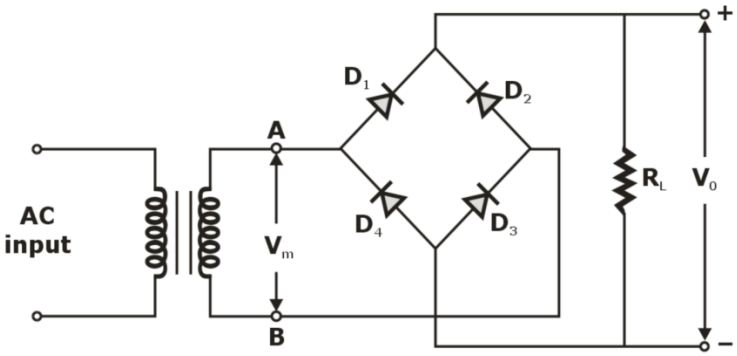


Figure 11: Bride Rectifier

10. FILTERS

A filter circuit is a device to remove the AC components of the rectified output, but allows the DC components to reach the load.

10.1 Capacitor filter:

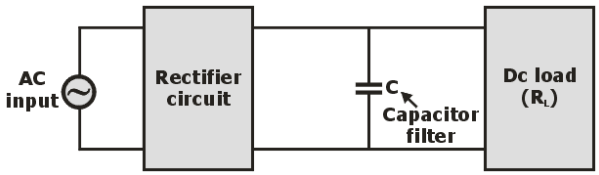


Figure 12: Basic capacitor filter circuit

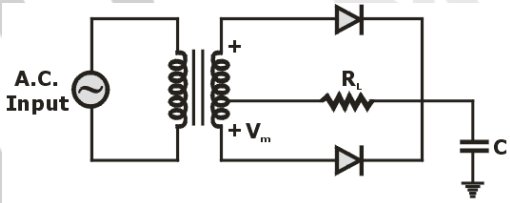


Figure 13(a): Full wave rectifier with capacitor filter

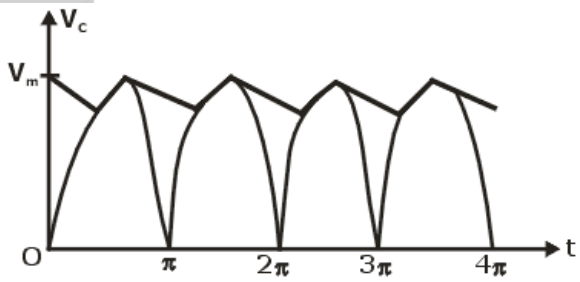


Figure 13 (b): Filtered output voltage

$$\boxed{r.f. = \frac{1}{4\sqrt{3}fCR_L}}$$

10.2 Inductive filter:

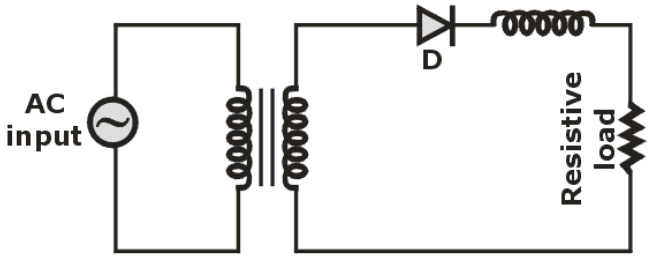


Figure 14: Inductive Filter circuit

$$\text{Ripple factor} = \frac{\sqrt{2}}{3} \cdot \frac{R_L}{2\omega L} \Rightarrow \frac{R_L}{3\sqrt{2}\omega L}$$

10.3 LC filter:

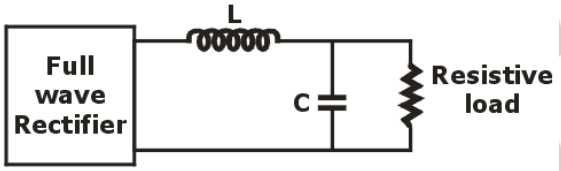


Figure 15: LC Filter circuit

Inductance is higher with respect to capacitance.

$$\boxed{\text{r.f.} = \frac{\sqrt{2}}{3}\frac{X_C}{X_L}}$$

10.4 π- section filter:

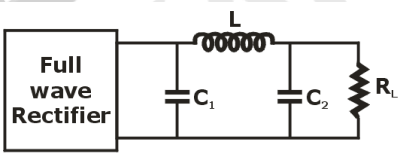


Figure 16: π – section filter circuit

$$\boxed{\text{ripple factor.} = \frac{\sqrt{2}\, X_{C_1} \cdot X_{C_2}}{X_L \cdot R_L}}$$

Here, X_{C1}, X_{C2}, X_L are reactance and R_L is resistive load.

10.5.RC filter :

RC filters are formed by replacing the inductor component of the π-section filter.

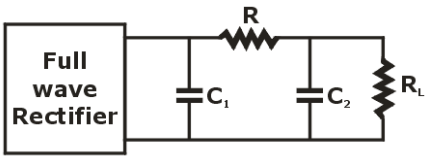


Figure 17: RC filter circuit

$$\boxed{\text{Ripple factor} = \frac{\sqrt{2}X_{C_1}X_{C_2}}{R \cdot R_L}}$$

CHAPTER 2:VOLTAGE REGULATORS

1.REGULATOR

i. The output resistance of the regulator should as low as possible, ideally zero.

ii. The maximum power dissipation by the Zener diode should be as low as possible.

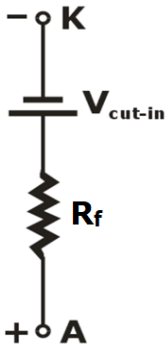
Forward Biased Zener Diode ($V_A > V_K$)	Ideal	Practical
		

Fig 1. Equivalent Circuit of Zener Diode

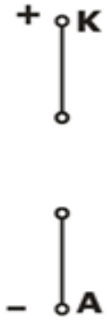
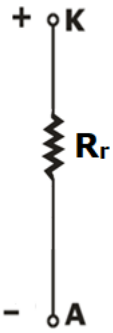
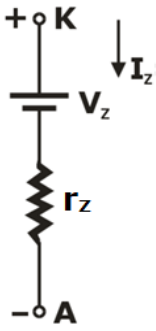
Reverse Biased Zener Diode ($V_A < V_K$)	Ideal	Practical
		
Breakdown Region Zener Diode ($V_K > V_Z$)	**Ideal**	**Practical**
		

Figure 2: Equivalent Circuit of Zener Diode

CHAPTER 3 : BJT BIASING & STABILIZATION

1. SIMPLIFIED STRUCTURE OF BJT AND MODE OF OPERATION:

Table-1

BJT Modes of operation		
Mode	**EBJ**	**CBJ**
Cut-off	Reverse	Reverse
Active	Forward	Reverse
Reverse Active	Reverse	Forward
Saturation	Forward	Forward

2.Relation between current gain :

For dc mode, common emitter current gain

$$\boxed{\beta = \frac{I_C}{I_B}}$$

And, common base current gain

$$\boxed{\alpha = \frac{I_C}{I_E}}$$

$$\boxed{\alpha = \frac{\beta}{\beta + 1}} \quad \& \quad \boxed{\beta = \frac{\alpha}{1 - \alpha}}$$

3.Calculation of Stability (S)

$$\boxed{S = \frac{\partial I_c}{\partial I_{co}} = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_c}}} \quad .....(xi)$$

- For any BJT circuit $\frac{\partial I_B}{\partial I_c}$ lies between 0 and –1. So, S lies between 1 and (1 + β)
- Since smaller stability factor is desired, so ideally Stability factor should be equal to 1.

4.BJT BIASING

4.1 Fixed Bias:

$$\boxed{S = 1 + \beta}$$

Disadvantage

- If β = 100, the stability factor is 101 and the collector current is 101 times that I_{CO}, reverse saturation current. Hence the stability factor for a fixed biased circuit is very high. So, it will be the least stable biasing arrangement.

4.2 Collector to base bias circuit :

$$S = \frac{\beta + 1}{1 + \beta\left(\frac{R_C}{R_C + R_B}\right)}$$

Advantage

- Stability factor is smaller than (β + 1), hence an improvement in stability is obtained over fixed bias circuit.

Disadvantage

- Stability factor depends upon R_C. If R_c becomes smaller or zero, then stability factor becomes very large and I_C does not remain stable.
- Resistance R_B connected from collector to base cause negative feedback due to which voltage gain of the amplifiers circuit decreases.

4.3. Self-bias or Voltage-Divider bias:

$$S = \frac{1 + \beta}{1 + \frac{\beta R_E}{R_b + R_E}}$$

Important point

- S varies between 1 for small R_b/R_E and $1 + \beta$ for $R_b/R_E \rightarrow \infty$
- Smaller value of R_b, better to stabilization

(Note: even if R_b becomes zero, the value of S can't be reduced below unity. Hence I_c always increases more than I_{co}.**)**

CHAPTER 4 : CURRENT MIRROR CIRCUITS

1.CURRENT MIRROR CIRCUIT

NOTE : for Current Mirror:

High output resistance
Low input resistance

1.1.Dc Analysis Of Bipolar Transistor Current Mirror

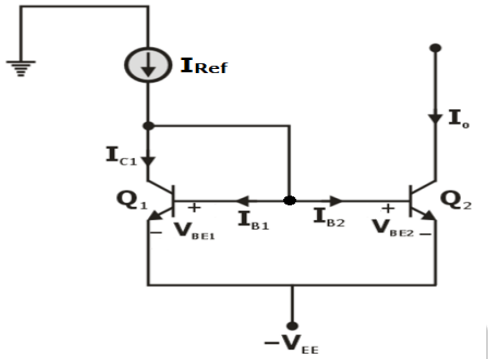


Figure 1

$$\therefore \text{Mirror Ratio} = MR = \frac{I_{C1}}{I_{Ref}} = \frac{1}{1+\frac{2}{\beta}}$$

NOTE : **Generalized Formula**

$$I_{C1} = \frac{I_R n}{1+\frac{n+1}{\beta}}$$

Here, n = no. of transistors.

1.2.Drawback Of Single Current Mirror

(a) The main drawback of a single Current Mirror is that the no. of transistors cannot be more than 10.

i.e., $I_0 = nI_{C1} = \frac{n \cdot I_R}{1+\frac{n+1}{\beta}}$ Here n = no. of transistors $n < 10$

(b) Single Current Mirror holds only for higher values of β.

(c) This Mirror concept is only used for perfectly matched transistors.

∴ we used Modified Current Mirror that can be used for n (no. of transistors) greater than 10 and β limitation is also removed.

2. MODIFIED CURRENT MIRROR: [n > 10]

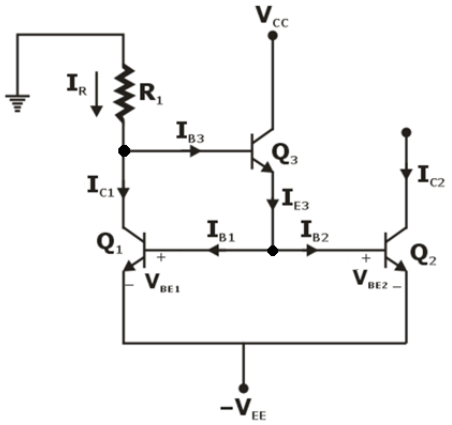


Figure 3

$$I_R = I_{C1}\left[1 + \frac{2}{\beta(1+\beta)}\right]$$

$$\therefore \boxed{I_{C1} = \frac{I_R}{1 + \frac{2}{\beta(\beta+1)}}}$$

<u>NOTE</u>: In General, for n current sources,

$$\boxed{I_C = \frac{I_R}{1 + \frac{n+1}{\beta(\beta+1)}}} \quad \text{for } n > 10$$

Applications of Current Mirror

(i) It can be used as a Current Regulator

(ii) It is used in biasing circuits

(iii) It is used is differential Amplifiers as a current source at the emitter terminal.

CHAPTER 5 : BJT AMPLIFIERS

1. HYBRID EQUIVALENT MODEL:

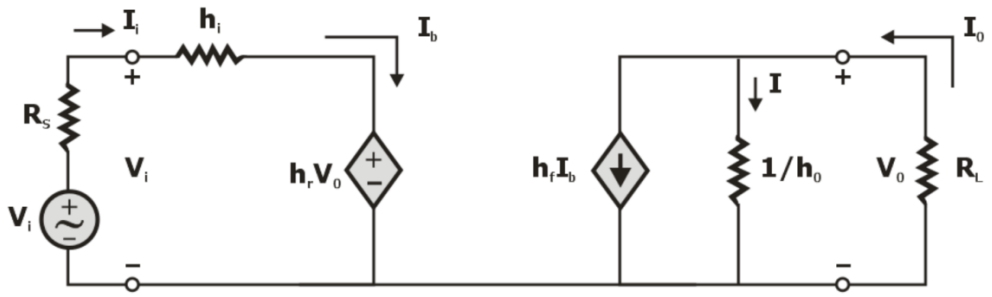


Figure 1: Hybrid equivalent Circuit

- $A_i = \frac{I_0}{I_i} = \frac{h_f}{1 + h_0R_L}$
- $A_V = \frac{V_0}{V_i} = -\frac{h_fR_L}{h_i + (h_ih_0 - h_fh_r)R_L}$
- $Z_i = \frac{V_i}{I_i} = h_i - h_rR_LA_i \qquad = h_i - h_rR_L\frac{h_f}{1 + h_0R_L}$
- $Z_0 = \frac{V_0}{I_0} = \frac{1}{h_0 - [h_rh_f(h_i + R_s)]}$

1.1 Summary of h-parameters:

Table-1 h-parameter for Common-Emitter Configuration

h-parameters	Expression
Input impedance	$h_{ie} = \left.\frac{\Delta V_{be}}{\Delta i_b}\right\|_{V_{CE}=\text{const}}$ ohms
Reverse voltage gain	$h_{re} = \left.\frac{\Delta V_{be}}{\Delta V_{ce}}\right\|_{I_B=\text{const}}$ unitless
Forward current gain	$h_{fe} = \left.\frac{\Delta i_c}{\Delta i_b}\right\|_{V_{CE}=\text{const}}$ unitless
Output conductance	$h_{oe} = \left.\frac{\Delta I_c}{\Delta V_{ce}}\right\|_{I_B=\text{const}}$ siemens

Table 2: Conversion table for Hybrid Parameters

Common-base to common-emitter	Common-emitter to common-base	Common-base to common-collector
$h_{ie} = \frac{h_{ib}}{1+h_{fb}}$	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$	$h_{ic} = \frac{h_{ib}}{1+h_{fb}}$
$h_{re} = \frac{h_{ib}h_{ob}}{1+h_{fb}} - h_{rb}$	$h_{rb} = \frac{h_{ie}h_{ob}}{1+h_{fe}} - h_{re}$	$h_{rc} = 1$
$h_{fe} = -\frac{h_{fb}}{1+h_{fb}}$	$h_{fb} = -\frac{h_{fe}}{1+h_{fe}}$	$h_{fc} = \frac{-1}{1+h_{fb}}$
$h_{oe} = \frac{h_{ob}}{1+h_{fb}}$	$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$	$h_{oc} = \frac{h_{ob}}{1+h_{fb}}$

Table 3: Typical values of h-parameters for CE, CC and CB Transistor Configurations

h-Parameters	Common-emitter	Common-collector	Common-base
h_i	1 kΩ	1 kΩ	20 Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	−50	−0.98
$1/h_0$	40 kΩ	40 kΩ	2 MΩ

2. Base Current and input Resistance at the Base :

The small signal input resistance between base and emitter, looking into the base, is denoted by $\mathbf{r_\pi}$ and is defined as

$$r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{V_T}{I_B} \quad \text{or} \quad r_\pi = \frac{\beta V_T}{I_C}$$

3.**Emitter Current and the input Resistance at the Emitter :**

$$r_e = \frac{v_{be}}{i_e} = \frac{V_T}{I_E} = \frac{r_\pi}{1+\beta}$$

4.SMALL SIGNAL HYBRID-Π EQUIVALENT CIRCUIT OF BJT:

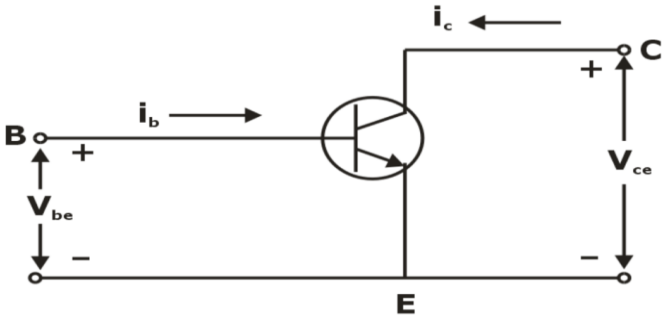


Figure 2

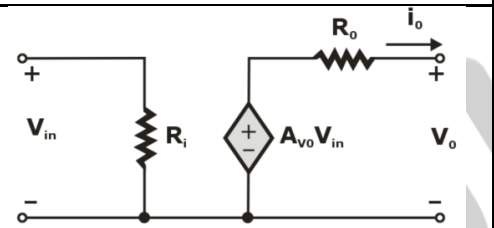
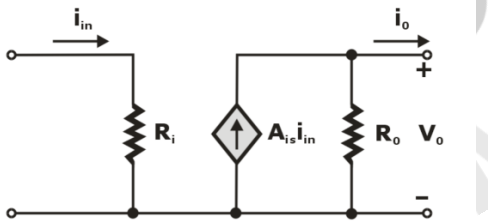
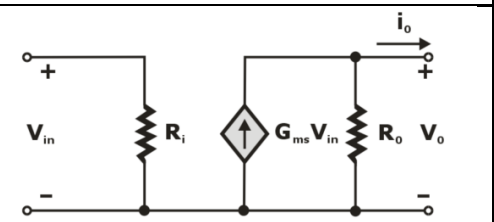
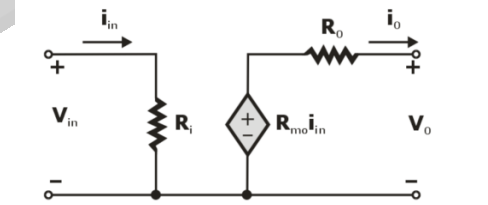
$$\frac{V_{be}}{i_b} = r_\pi = \frac{V_T}{I_{BQ}} = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

$$r_\pi g_m = \frac{\beta V_T}{I_{CQ}} \cdot \frac{I_{CQ}}{V_T} = \beta$$

5.BASIC TRANSISTOR AMPLIFIER CONFIGURATIONS :

Table 4

Four equivalent two-ports network		
Gain Property	**Equivalent circuit**	**Gain Property**
Voltage amplifier		Output voltage proportional to input voltage
Current amplifier		Output current proportional to input current
Transconductance amplifier		Output current proportional to input voltage
Transresistance amplifier		Output voltage proportional to input current

6.Different Types of Amplifiers comparison:

Table 5: Different Types of Amplifiers & its performance parameters

	Voltage Gain A_V	Input Impedance	Output Impedance	Current Gain A_I
Common Emitter with R_E	$\frac{\beta}{r_\pi}R_L'' = g_m R_L''$ $\left(R_L'' = r_o \,\|\|\, R_C \,\|\|\, R_L\right)$	$R_i = r_\pi \,\|\|\, R_B$ $R_i' = R_S + (R_i)$	$r_o \,\|\|\, R_C$	$\frac{-\beta R_C'}{R_C' + R_C}$ $\left(R_C' = R_C \,\|\|\, r_o\right)$
Common Emitter without R_E	$\frac{\beta R_L''}{r_\pi + (1+\beta)R_E} = \frac{-g_m R_L''}{1 + g_m R_E}$	$R_i = r_\pi + (1+\beta)R_E$ $R_i' = R_s + R_i$	R_C	$-\beta$
Common Collector	$\frac{(1+\beta)R_E''}{r_\pi + (1+\beta)R_E''} \approx 1$ $\left(R_E'' = R_E \,\|\|\, r_o\right)$	$R_i = r_\pi + (1+\beta)R_E'$ $R_i' = (R_S \,\|\|\, R_B) + R_i$	$R_E \,\|\|\, r_o \,\|\|\, \left[\frac{R_S + r_\pi}{(1+\beta)}\right]$	$\frac{(\beta+1)r_o}{(R_E + r_o)} \approx (\beta+1) \approx \beta$
Common Base	$\frac{\beta}{r_\pi}(R_C \,\|\|\, R_C) = g_m (R_C \,\|\|\, R_L)$	$\frac{r_\pi}{1+\beta}$	R_C	$\frac{g_m R_C}{R_C + R_L}\left(\frac{r_\pi}{(1+\beta)} \,\|\|\, R_E\right) \approx 1$

7. FREQUENCY RESPONSE OF COMMON EMITTER AMPLIFIER:

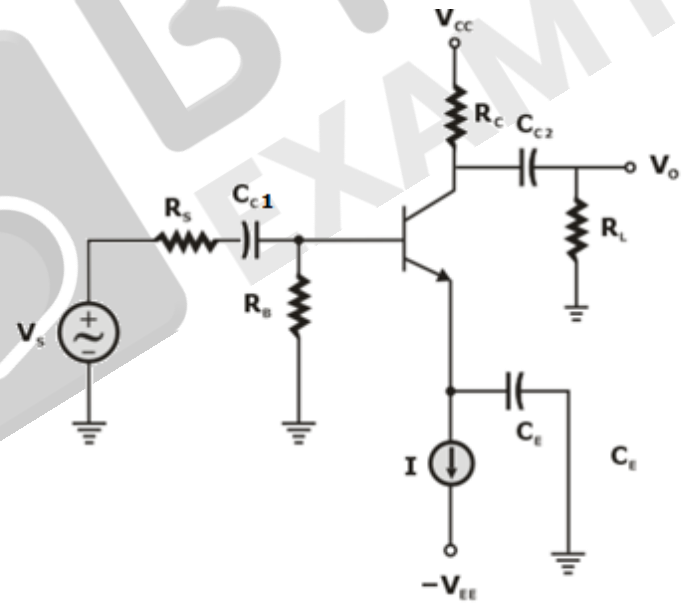


Figure 3: Capacitive Coupled Common Emitter Amplifier

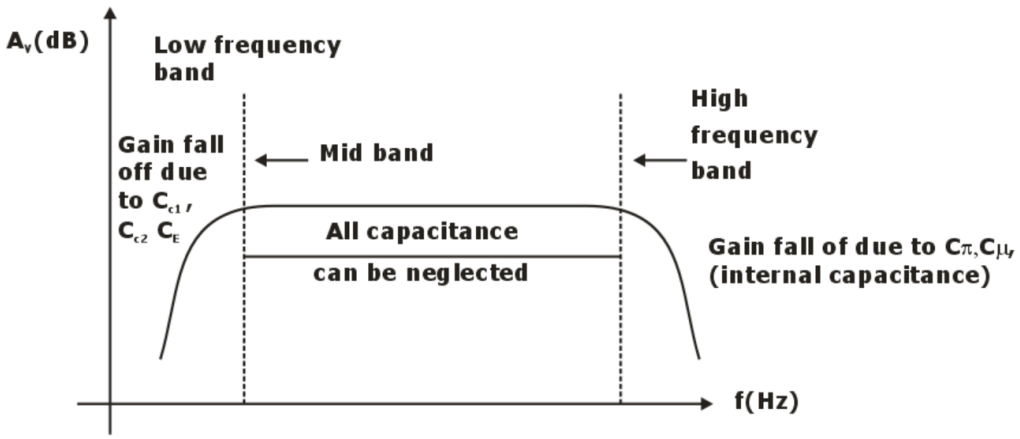


Figure 4: Magnitude of gain of the CE amplifier versus frequency

7.1. Cut-off Frequency

For a given circuit with equivalent resistance (R_{eq}) and equivalent capacitance (C_{eq}), the 3-dB cut-off frequency is given by

$$f_{3dB} = \frac{1}{2\pi C_{eq} R_{eq}}$$

Thus, we calculate 3 dB frequencies due to C_{C1}, C_{C2}, C_E as below.

- The effect of C_{C1} is determined with C_E and C_{C2} assumed to be acting as perfect short circuit as shown in fig, So,

$$(f_{3dB})_{C_{C1}} = \frac{1}{2\pi C_{C1}((R_B \,||\, r_\pi) + R_S)}$$

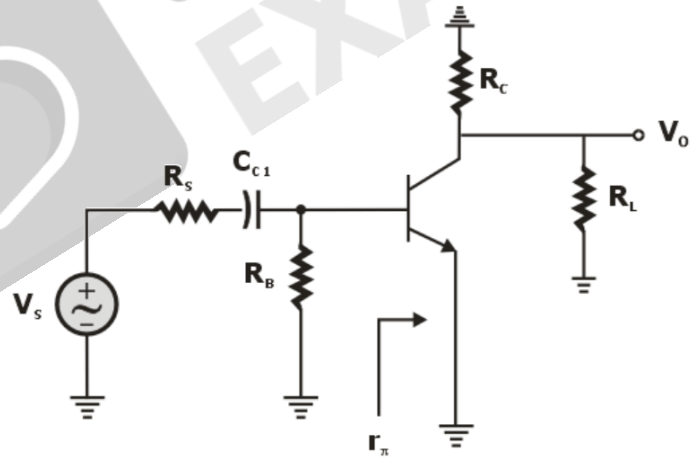


Figure 5 :The effect of C_{c1} is determined with C_E and C_{c2} assumed to be acting as perfect short circuit

- The 3 dB frequency due to C_{C2} is given by

$$(f_3dB)_{C_{C2}} = \frac{1}{2\pi C_{C2}(R_C + R_L)}$$

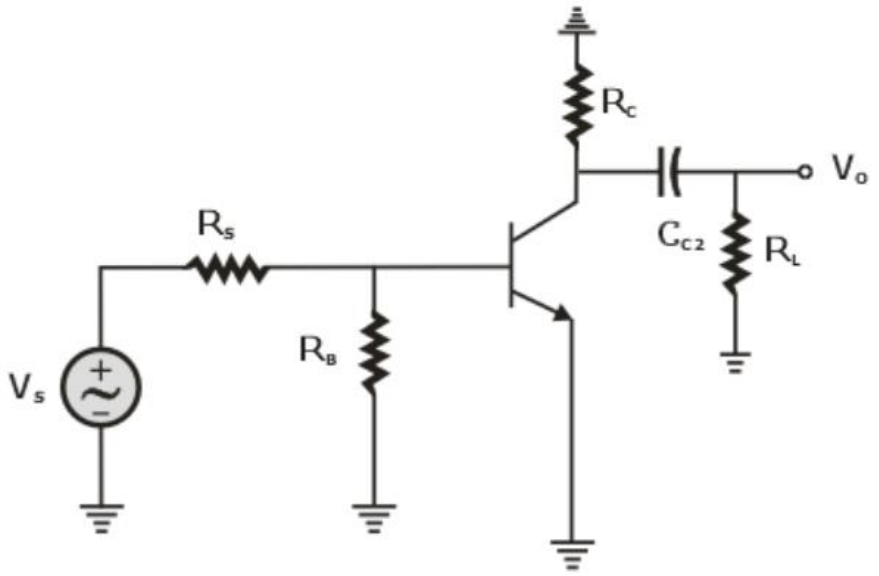


Figure 6 :The effect of C_{c2} is determined with C_{c1} and C_E assumed to be as perfect short circuit.

- The 3 dB frequency due to C_E is given by

$$\left(f_{3dB}\right)_{C_E} = \frac{1}{2\pi C_E\left(r_e + \frac{R_B \,||\, R_S}{\beta + 1}\right)}$$

CHAPTER 6 : MOSFET Biasing & Amplifiers

1.MOS TRANSCONDUCTANCE:

1.1.Transconductand in saturation region:

$$I_{D(sat)} = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{th})^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})$$

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \sqrt{2KI_D}$$

1.2 **Various dependencies of g_m**

Table 1

$\frac{W}{L}$ constant $V_{GS}-V_{TH}$ variable	$\frac{W}{L}$ variable $V_{GS}-V_{TH}$ constant	$\frac{W}{L}$ variable $V_{GS}-V_{TH}$ constant
$g_m \alpha \sqrt{I_D}$	$g_m \propto \sqrt{I_D}$	$g_m \propto \sqrt{\frac{W}{L}}$
$g_m \propto V_{GS} - V_{TH}$	$g_m \propto \frac{W}{L}$	$g_m \propto \frac{1}{V_{GS} - V_{TH}}$

2. DIFFERENT BIASING METHODS

2.1 Drain to gate bias configuration:

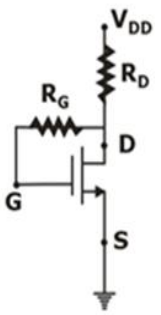


Figure 5.a: Drain to bias configuration,

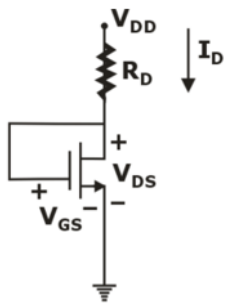


Figure 5.b : DC equivalent

$$\boxed{V_{DS} = V_{GS}}$$

Drain to gate bias always enables MOSFET in saturation region

2.2 Fixed bias configuration:

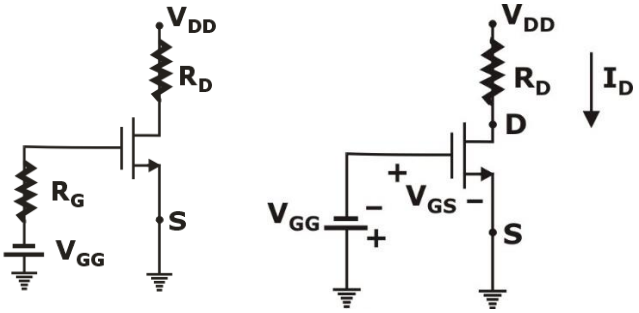


Figure 2 (a) and (b)

<u>DRAWBACK OF FIXED BIAS:</u>

It is a dual battery design which makes it expensive and more space occupied bias Configuration.

2.3 Self bias configuration:

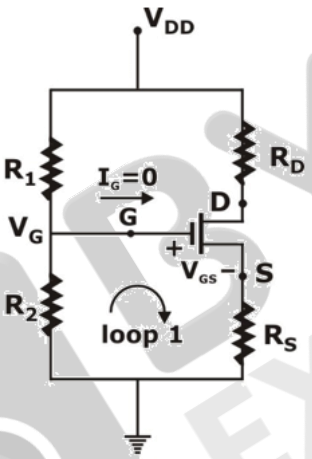


Figure 5.c: Voltage divider configuration,

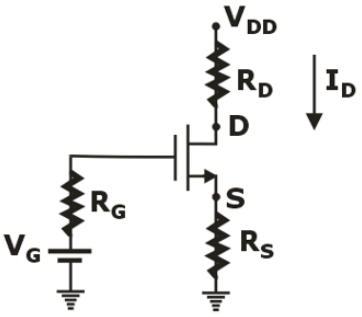


Figure 5.d: DC Equivalent

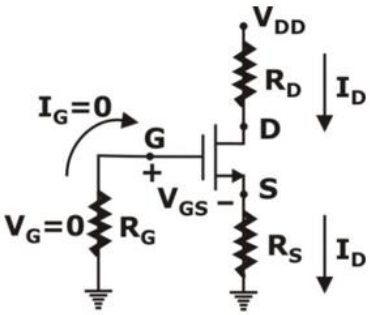


Figure 5.e : DC equivalent

$$\therefore (I_D)_Q = -\frac{(V_{GS})_Q}{R_S}$$

Vds= Vdd-Id(Rs+Rd)

3.SMALL SIGNAL AC EQUIVALENT MODEL

- Comparison between BJT and MOSFET:

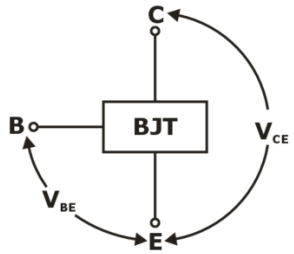
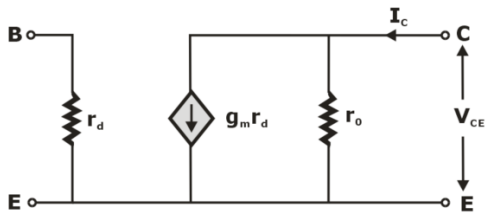
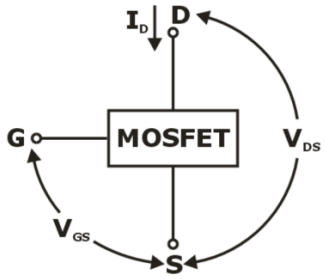
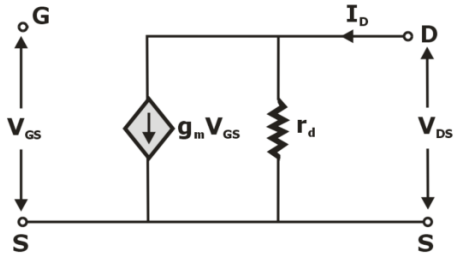
BJT	MOSFET
 Current Controlled Current Source (CCCS)  Here, g_m = transconductance r_d = dynamic resistance r_o = output resistance ∴ In BJT, high input impedance and low output impedance Therefore, BJT = CCCS ⇒ **Current amplifier**	 Voltage Controlled Current Source (VCCS)  Here, g_m = transconductance r_d = dynamic resistance $I_D = f(V_{GS}, I_{DS})$ $I_D = \underbrace{\frac{\partial I_D}{\partial V_{GS}}}_{g_m} \cdot V_{GS} + \underbrace{\frac{\partial I_D}{\partial V_{DS}}}_{1/r_d} \cdot V_{DS}$ Therefore, MOSFET = VCCS ⇒ **Transconductance amplifier**

Table 2: Comparison between BJT and MOSFET

4.ANALYSIS OF COMMON SOURCE AMPLIFIER

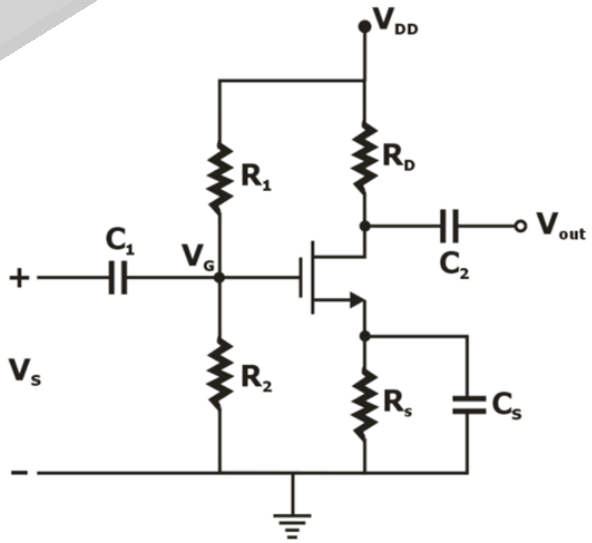


Figure 2 : CS Configuration of E-MOSFET with potential divider biasing (Bypassed Rs)

PARAMETER	EXACT	With $r_d >> R_D$
Z_I	R_G	R_G
Z_O	$R_D \| \| r_d$	R_D
A_V	$-g_m(R_D \| \| r_d)$	$-g_m R_D$

Table 2: Summarized performance of common source amplifier

5.ANALYSIS OF COMMON DRAIN AMPLIFIER:

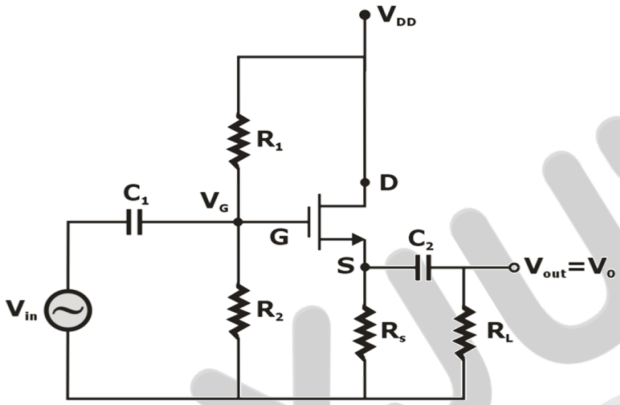


Figure 3: Circuit diagram of Common Drain Amplifier

PARAMETER	EXACT	$r_d >> R_D$
Z_I	R_G	R_G
Z_0	$\frac{1}{g_m} \| \| R_S$	$\frac{1}{g_m} \| \| R_S$
A_V	$\frac{g_m (r_d \| \| R_s)}{1 + g_m (r_d \| \| R_s)}$	$\frac{g_m R_s}{1 + g_m R_s}$

Table 3: Summarized performance of Common Drain Amplifier

6. ANALYSIS OF COMMON GATE AMPLIFIER

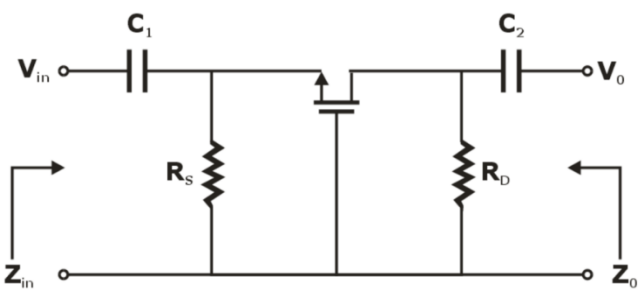


Figure 5: Common Gate Amplifier

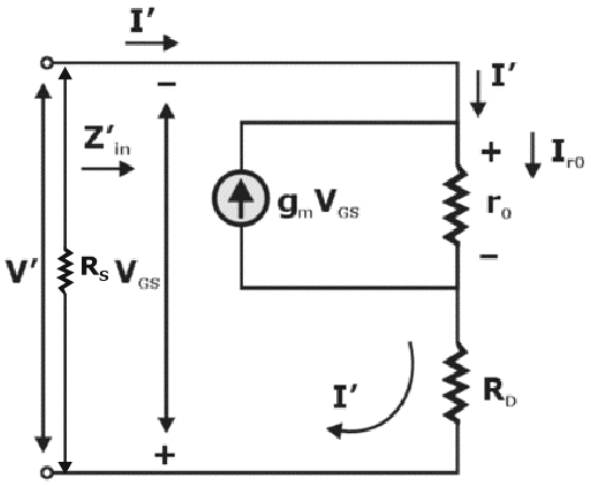


Figure 6: Simplified small signal model

$$Z_{in}' = \frac{(r_0 + R_D)}{(1 + g_m r_0)}$$

$$Z_{in} = \left(R_S \,||\, \frac{1}{g_m}\right) \qquad \text{(if } r_0 \text{ is infinity)}$$

$$Z_0 = R_D \,||\, r_0$$

$$Z_0 = R_D \qquad \text{(if } r_0 \text{ is infinity)}$$

$$A_v = \frac{V_0}{V_{in}} = \left[\frac{\left(g_m R_D + \frac{R_D}{r_0}\right)}{\left(1 + \frac{R_D}{r_0}\right)}\right]$$

$$\boxed{\text{Voltage gain} = A_v = g_m R_D}$$

CHAPTER 7 : MULTI STAGE AMPLIFIERS

1.Cascading Amplifier

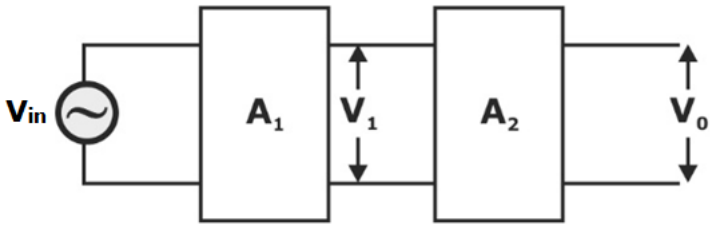


Figure 1: Two stage Amplifier.

$$A = A_1 \times A_2$$

$$\boxed{A = \frac{V_0}{V_{in}}}$$

2.EFFECT OF CASCADING ON BANDWIDTH

2.1. Identical Stages:

The lower cutoff frequency for the multi stage amplifier is given by :

$$\boxed{(f_C)_{low} = \frac{f_L}{\sqrt{2^{1/n} - 1}}}$$

and the upper cutoff frequency for multi-stage amplifier is given by:

$$\boxed{(f_C)_{high} = f_H \cdot \sqrt{2^{1/n} - 1}}$$

Here,

n = no. of stages

f_L, f_H are low & high frequency respectively.

Thus, bandwidth of multi-stage amplifier is $Bw = (f_C)_{high} - (f_C)_{low}$

2.2.Non-Identical stages:

Here for every gain, separate bandwidth is present.

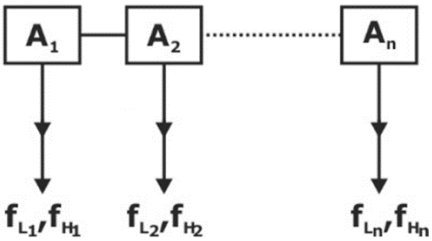


Figure 2: Cascading of non-identical stages

$$\therefore \quad \boxed{f_L^n = 1.1\sqrt{f_{L_1}^2 + f_{L_2}^2 + \ldots f_{Ln}^2}}$$

Similarly, $$f_H^n = \frac{1.1}{\sqrt{\frac{1}{f_{H_1}^2} + \frac{1}{f_{H_2}^2} \cdots \frac{1}{f_{H_n}^2}}}$$

3.EFFECT OF CASCADING ON RISE TIME (t_r)

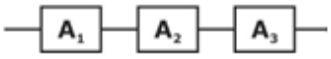
3.1. For Single Stage:

$$t_r = \frac{0.35}{f_H}$$

Here, t_r = rise-time

f_H = bandwidth

3.2. For Multi Stage:



$$t_r = 1.1\sqrt{t_{r1}^2 + t_{r2}^2 + t_{r3}^2}$$

∴ Rise time of Multistage:

Conclusion:

(i) Bandwidth of multi-stage amplifier is always **less** than bandwidth of single stage amplifier (Gain = more)

(ii) Rise-time of multi-stage amplifier is always **greater** than rise time of single stage amplifier.

4.Comparison of different type of coupling :

Table 1

Characteristic	R-C coupling	Transformer coupling	Direct Coupling
Frequency Response	Excellent in audio frequency range	Poor	Best
Cost	Less	More	Least
Space & Weight	Less	More	Least
Impedance Matching	Not good	Excellent	Good
Use	Voltage amplification	Power amplification	amplifying extremely low frequency

5. POPULAR CASCADING DESIGN:

5.1.1 Cascade Amplifier: (CE – CB configuration)-

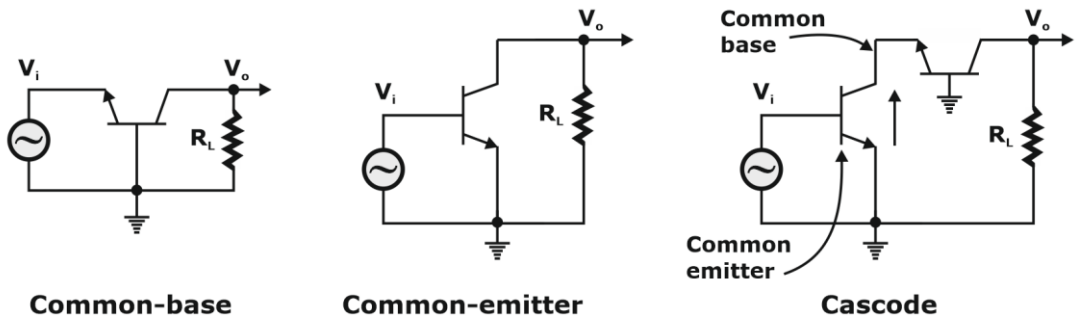


Figure 3: Cascode Amplifier Configuration

cascode amplifier has a high gain, moderately high input impedance, a high output impedance, and a high bandwidth.

5.1.2 **Transconductance of below cascode amplifier:**

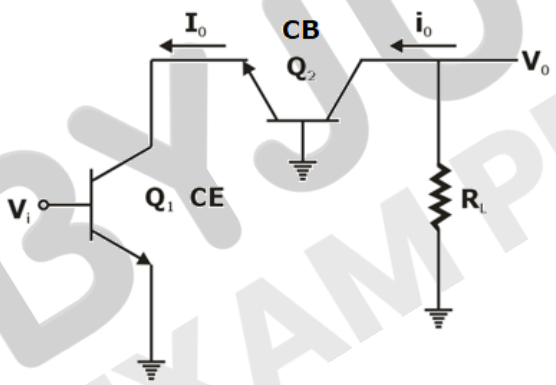


Figure 4: Cascode Amplifier

$$(g_m)_{cascode} = g_{m_1}$$

5.2 Darlington Pair [CC – CC]

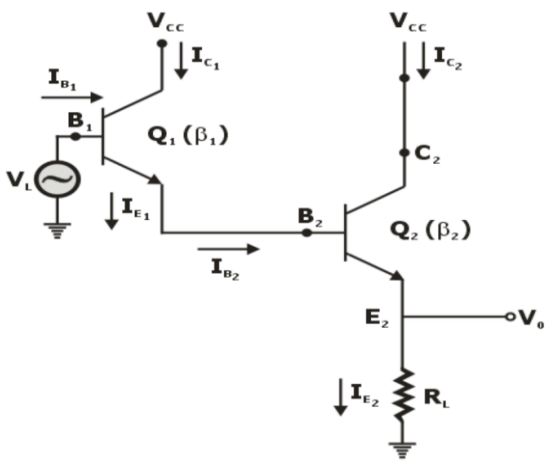


Figure 5: Darlington pair configuration

5.3 DIFFERENCE:

Emitter Follower	Darlington pair
 (i) $A_I = \beta$ (ii) $A_V = 1$ (CC = voltage buffer) (iii) $Z_i = \beta R_L$ (iv) $Z_0 = r_e$	 $A_I = A_{I1} \cdot A_{I2}$ $A_I = \frac{I_{E1}}{I_{B1}} \cdot \frac{I_{E2}}{I_{B2}}$ $A_I = \frac{(1+\beta_1)I_{B1}}{I_{B1}} \cdot \frac{(1+\beta_2)I_{B2}}{I_{B2}}$ $\boxed{A_I = (1+\beta_1) \times (1+\beta_2)}$ $\therefore \boxed{\text{overall } \beta \approx \beta_1 \cdot \beta_2}$ (ii) $Z_i = (1+\beta_1)(1+\beta_2)R_L \approx \beta_1\beta_2 R_L$

Table 3: Difference between Emitter follower and Darlington pair

Following are the important characteristics of Darlington pair:

- Extremely high input impedance.
- Extremely high current gain.
- Extremely low output impedance.

CHAPTER 8: FEEDBACK AMPLIFIERS

1. Difference between positive and negative feedback:

Positive feedback	Negative feedback
$V_0 = A_{Vi}$	$V_0 = A_{Vi}$
$V_i = V_s + V_f$	$V_i = V_s - V_f$
$V_0 = A(V_s + V_f)$	$V_0 = A(V_s - V_f)$
$V_0 = A(V_s + \beta V_0)$	$V_0 = A(V_s - \beta V_0)$
$V_0(1 - \beta A) = AV_S$	$V_0(1+ \beta A) = AV_S$
$\frac{V_0}{V_s} = \frac{A}{1 - A\beta}$	$\frac{V_0}{V_s} = \frac{A}{1 + A\beta}$

Table 1: Difference between positive and negative feedback

1.1 Conclusion

(1) $A_{pf} > A > A_{nf}$.

(2) $A_{nf} = \frac{A}{1+\beta A}$ $\beta A >>> 1$

$A_{nf} = \frac{1}{\beta}$ stability.

NOTE- Negative feedback theory is applied for stable system like Amplifier.

(3) $A_{pf} = \frac{A}{1-\beta A}$

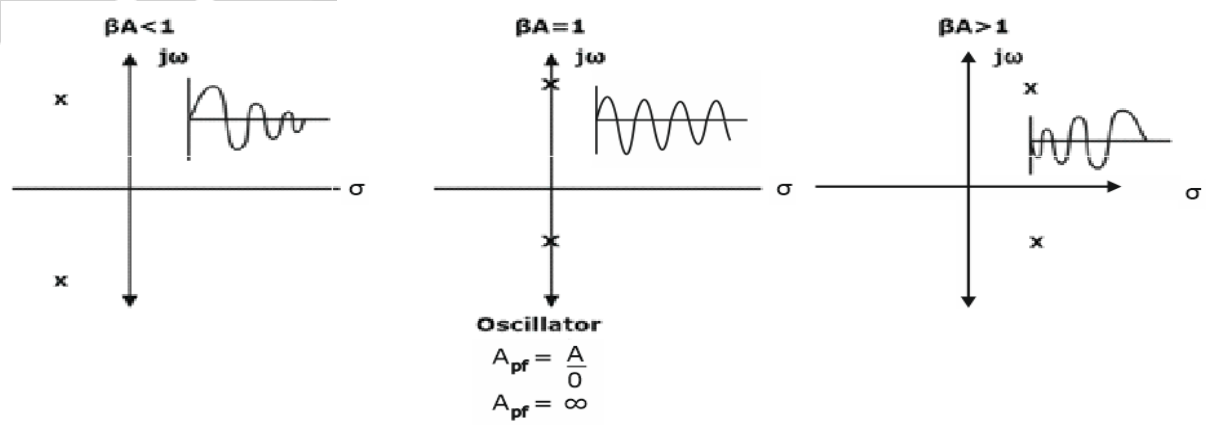


Figure 1

NOTE- Positive feedback theory is applied for unstable system like oscillator

2. EFFECTS OF NEGATIVE FEEDBACK

2.1 Advantage of Negative feedback amplifier

$$A_f = \frac{A}{1 + A\beta}$$

$$\frac{\partial A_f}{A_f} = \frac{\partial A}{A} \frac{1}{(1+BA)}$$

Fractional change of gain with feedback

Fractional change of gain with without feedback

$$\frac{\partial A_f / A_f}{\partial A_f / A} = \frac{1}{1 + \beta A} \Rightarrow \text{sensitivity}$$

$(1 + \beta A) \rightarrow$ desensitivity

2.2 Increase in input impedance

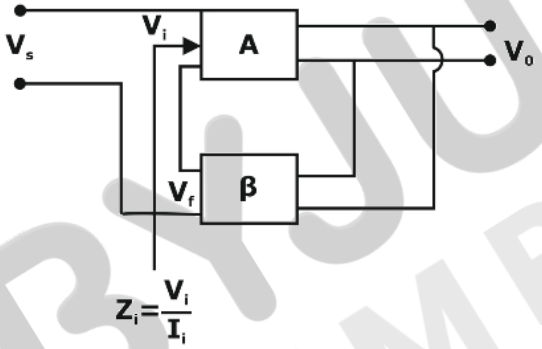


Figure 2

$$Z_{if} = Z_i (1 + A\beta)$$

2.3 Decrease in output impedance

$$Z_{of} = \frac{Z_0}{1 + \beta A}$$

2.4 Increase in BW

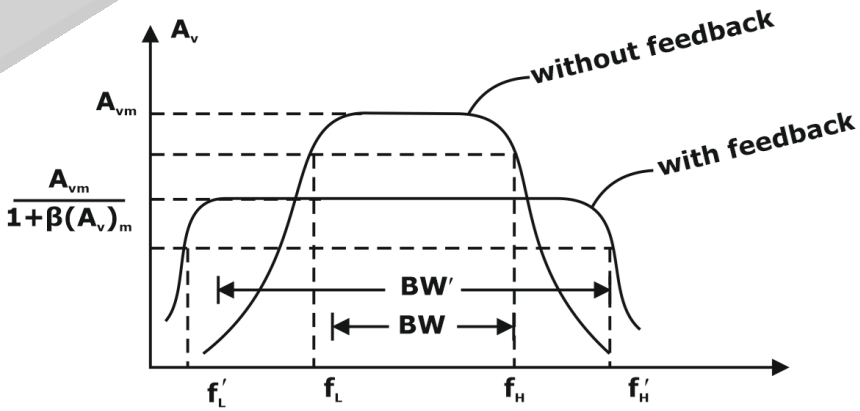


Figure 3

Lower cutoff frequency decreases

$$f'_L = \frac{f_L}{1 + A\beta}$$

Upper cutoff frequency increases

$$f'_H = (1 + A\beta) f_H$$

$$BW' = BW(1 + A\beta)$$

3.TOPOLOGY

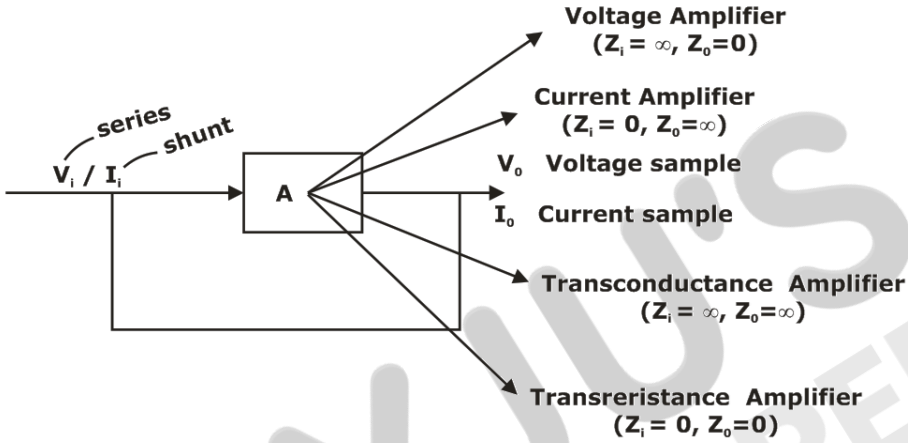


Figure 4-Block diagram analysis

3.1 At input side

At input side voltage mixed in series and current mixed in shunt.

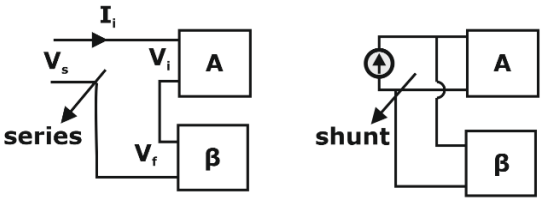


Figure 5

3.2 At output side

In output side current sampled in series and voltage sampled in shunt.

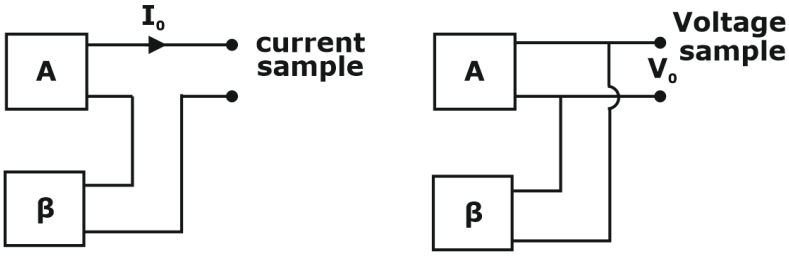


Figure 6

4.Amplifier Characteristics-

The **amplifier characteristics** which are affected by various negative feedback are listed in the following table 2

Amplifier	Nomenclature	Input Impedance	Output Impedance
Voltage Amplifier	Voltage series OR Series voltage OR Series shunt OR Voltage Voltage	$Z_i = \infty$ Increases $Z_{if} = Z_i (1 + A\beta)$	$Z_0 = 0$ Decreases
Transreistance Amplifier	Voltage shunt OR Shunt voltage OR Shunt shunt OR Voltage current OR	$Z_i = 0.$ Decrease $\frac{Z_i}{1+A\beta}$	$Z_0 = 0.$ Decrease $\frac{Z_0}{1+A\beta}$
Transconductance Amplifier	Current series OR Series current OR Series series OR Current voltage	$Z_i = \infty$ Input impedance increases $Z_i (1 + A\beta)$	$Z_0 = \infty$ output impedance increases $Z_0(1 + A\beta)$
Current Amplifier	Current shunt or Shunt Current or Shunt series or Current Current	Input impedance decreases $Z_i = 0$ $\frac{Z_i}{1+A\beta}$	output impedance increases $Z_0 = \infty$ $Z_0(1 + A\beta)$

Table 2

5.TYPES OF NEGATIVE FEEDBACK AMPLIFIERSRS:

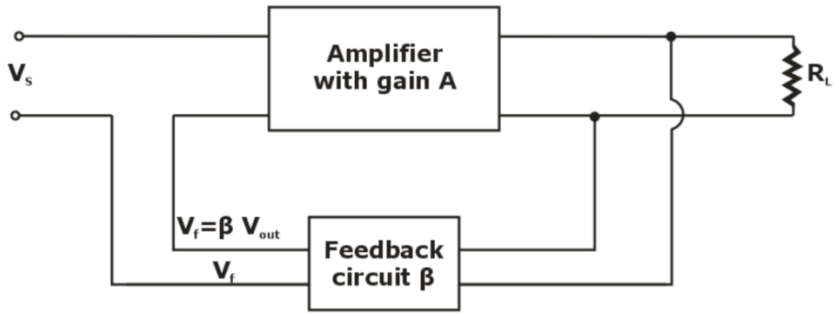


Figure 4.1: Voltage Series Topology

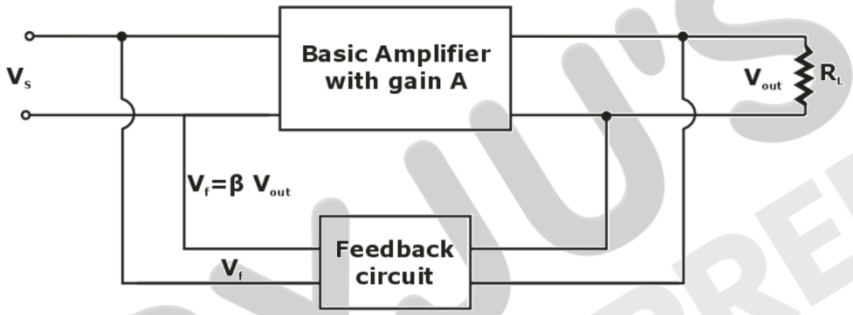


Figure 4.2 : Voltage Shunt Topology

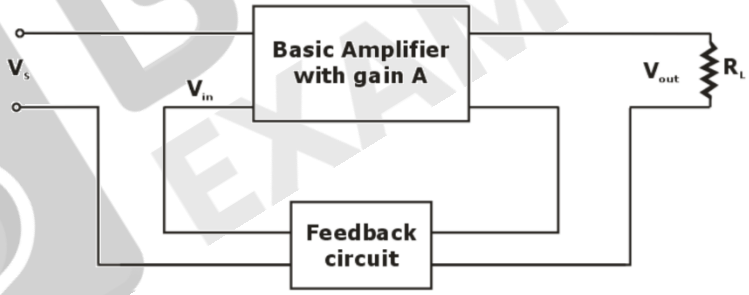


Figure 4.3 : Current Series Topology

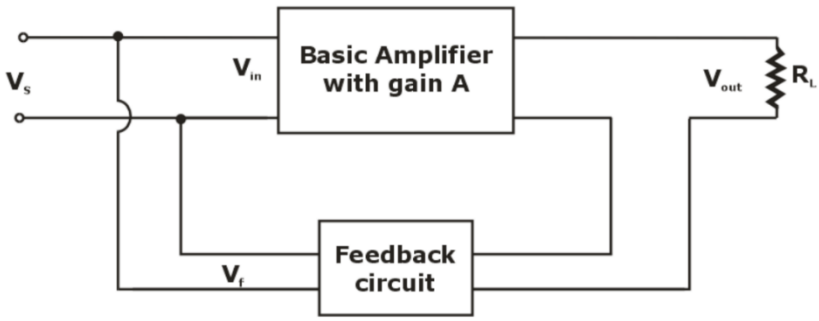


Figure 4.4: Current Shunt Topology

CHAPTER 9 :POWER AMPLIFIERS

1. BASICS OF POWER AMPLIFIERS

1.1.CLASS A POWER AMPLIFIERS

P_{in} = voltage × current = $V_{CC}(I_C)_Q$

$$(P_{out})_{ac} = I^2R_C = \frac{V^2}{R_C} = \left(\frac{V_m}{\sqrt{2}}\right)^2 \frac{1}{R_C} = \frac{V_m^2}{2R_C}$$

I = RMS value of ac output current through load.

V = RMS value of ac voltage

Overall efficiency (η):

$$\boxed{(\eta)_{overall} = \frac{(P_{out})_{ac}}{(P_{in})_{dc}}}$$

Here,

$(\eta)_{overall} \approx 30\%$

Transformer coupled class A power Amplifier: -

$$(\eta)_{collector} = \frac{V_{CC} \times (I_C)_Q}{2V_{CC} \times (I_C)_Q} = \frac{1}{2}$$

$$\eta = \frac{1}{2} \times 100\% = 50\%$$

CONCLUSION:

Therefore, the efficiency of class A power amplifier is nearly to 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

1.2. CLASS B POWER AMPLIFIERS:

POWER EFFICIENCY OF CLASS B PUSH PULL AMPLIFIER

$$(\eta)_{overall} = \frac{(P_{out})_{ac}}{(P_{in})_{dc}}$$

$$= \frac{\pi}{4} = 0.785 = 78.5\%$$

1.3. CLASS AB AMPLIFIER

The conduction angle of class AB amplifier is somewhere between 180° to 360° depending upon the operating point selected.

Efficiency of class AB is in between 50-60%

1.4. CLASS C AMPLIFIERS

The conduction angle for class C is less than 180°

2.COMPARISON

	Class A	Class B	Class AB	Class C
Efficiency	50%	78.5%	Between A & B	100%
Conduction angle	360°	180°	180°-220° (Greater than 180°)	100°-150° (less than 180°)

Table 1: Comparative study between different Power Amplifiers

CHAPTER 10 : DIFFERENTIAL AMPLIFIERS

1. Basics of Differential Amplifier:

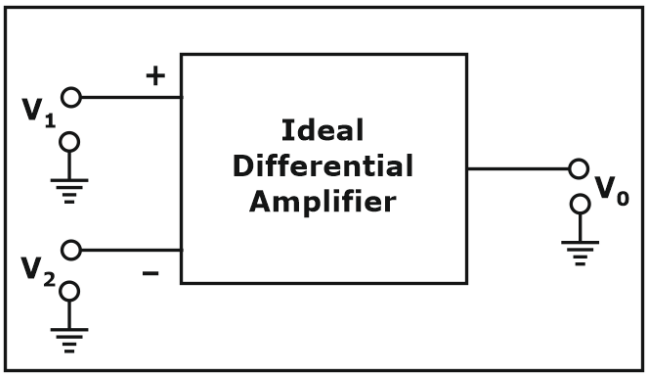


Fig. 1 Ideal differential amplifier

The differential amplifier amplifies the difference between two input voltage signals. Hence it is also called difference amplifier.

$V_o \propto (V_1 - V_2)$

2. Differential Gain (A_d)

$V_o = A_d(V_1 - V_2)$

Where, A_d = differential gain

The difference between the two inputs ($V_1 - V_2$) is generally called difference voltage and denoted as V_d.

$V_o = A_d V_d$

Hence, the differential gain can be expressed as,

$$A_d = \frac{V_o}{V_d}$$

Generally, the differential gain is expressed in its decibel (dB) value as,

$A_d = 20 \text{ Log}_{10} (A_d)$ in dB

3. Common Mode Gain (A_c):

The output voltage of the practical differential amplifier also depends on the average common level of the two inputs. Such an average level of the two input signals is **called common mode signal** denoted as V_c.

$$\therefore \quad V_c = \frac{V_1 + V_2}{2}$$

The gain with which it amplifies the common mode signal to produce the output is called **as common mode gain** of the differential amplifier denoted as A_c.

$\therefore \quad V_o = A_c V_c$

So, the total output of any differential amplifier can be expressed as,

$\therefore \quad V_o = A_d V_d + A_C V_c$

4. Common Mode Rejection Ratio (CMRR)

`The ability of a differential amplifier to reject a common mode signals is expressed by a ratio called **common mode rejection ratio** denoted as CMRR.

It is defined as the ratio of the differential voltage gain A_d to common mode voltage gain A_c.

$$\therefore \quad \text{CMRR} = \rho = \left|\frac{A_d}{A_c}\right|$$

*Ideally the common mode voltage gain is zero, hence the ideal value of CMRR is inifinite.

*For a practical differential amplifier A_d is large and A_c is small hence the value of CMRR is also very large.

*Many a times, CMRR is also expressed in dB, as

$$\text{CMRR in dB} = 20 \log \left|\frac{A_d}{A_c}\right| \text{dB}$$

The output voltage can be expressed in terms of CMRR as below:

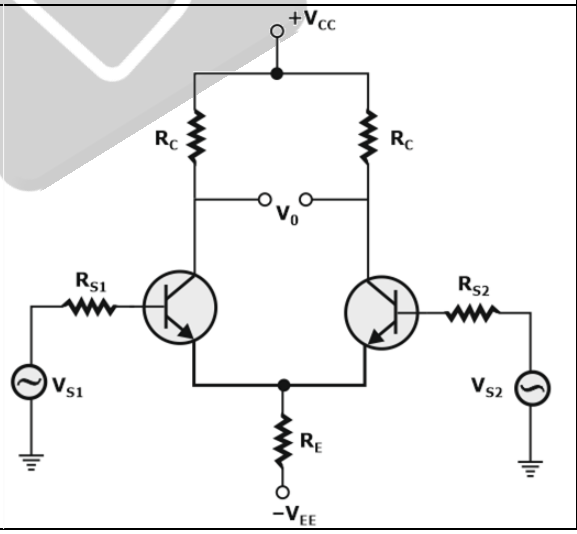
$$\therefore \quad V_o = A_d V_d + A_c V_c$$

$$= A_d V_d \left[1 + \frac{A_c V_c}{A_d V_d}\right]$$

$$\therefore \quad V_o = A_d V_d \left[1 + \frac{1}{\left(\frac{A_d}{A_c}\right)} \frac{V_c}{V_d}\right]$$

$$\therefore \quad V_o = A_d V_d \left[1 + \frac{1}{\text{CMRR}} \cdot \frac{V_c}{V_d}\right]$$

5. Different types of Differential Amplifier:

Configuration		Circuit	A_d Voltage gain	R_E Input resistance	R_0 Output resistance
1.	Dual Input, Balanced Output		$\frac{h_{fe} R_C}{R_S + h_{ie}}$	$2(R_S + h_{ie})$	R_C

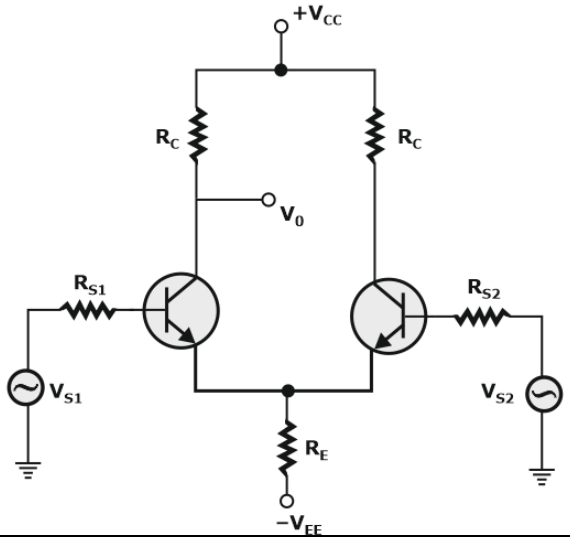
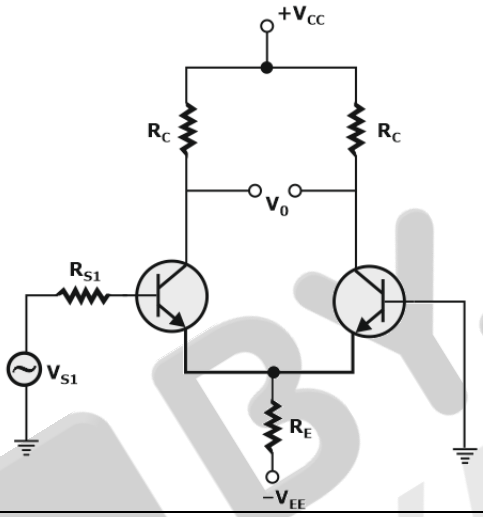
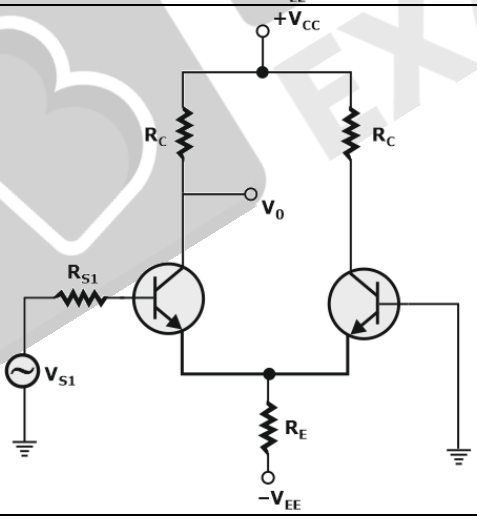
2.	Dual Input, Unbalanced Output		$\frac{h_{fe} R_C}{2(R_S + h_{ie})}$	$2(R_S + h_{ie})$	R_C
3.	Single Input, Balanced Output		$\frac{h_{fe} R_C}{R_S + h_{ie}}$	$2(R_S + h_{ie})$	R_C
4.	Single Input, Unbalanced Output		$\frac{h_{fe} R_C}{2(R_S + h_{ie})}$	$2(R_S + h_{ie})$	R_C

Table 5

The expression for the common mode gain A_c remains same for all the configurations which is,

$$A_c = \frac{h_{fe} R_C}{R_S + h_{ie} + 3R_E (1 + h_{fe})}$$

CHAPTER 11 : OPERATIONAL AMPLIFIERS

1. OPAMP INTRODUCTION:

1.1 COMPARISON BETWEEN IDEAL OPAMP AND PRACTICAL OPAMP:

Property	Ideal	Practical (Typical)
Open-loop gain	Infinite	Very high (>1000)
Open-loop bandwidth	Infinite	Dominant pole (≅ 10 Hz)
CMRR	Infinite	High (> 60 dB)
Input Resistance	Infinite	High (> 1 MΩ)
Output Resistance	Zero	Low (< 100 Ω)
Input Bias Currents	Zero	Low (< 50 nA)
Offset Voltages	Zero	Low (< 10 mV)
Offset Currents	Zero	Low (< 50 nA)
Slew Rate	Infinite	A few V/μs
Drift	Zero	Low

Table1: Comparison of an ideal and a typical practical opamp

1.2. Slew-Rate:

$$SR = \frac{\Delta V_0}{\Delta t} \text{ V/}\mu\text{s}$$

$$SR = A_{CL} \frac{\Delta V_i}{\Delta t}$$

1.3. Maximum Signal Frequency in terms of Slew Rate:

$$\boxed{f \le \frac{SR}{2\pi k} \text{ Hz}}$$

2. APPLICATIONS OF OP-AMP

2.1. Inverting-Amplifier:

$$A_v = \frac{-R_f}{R_1}$$

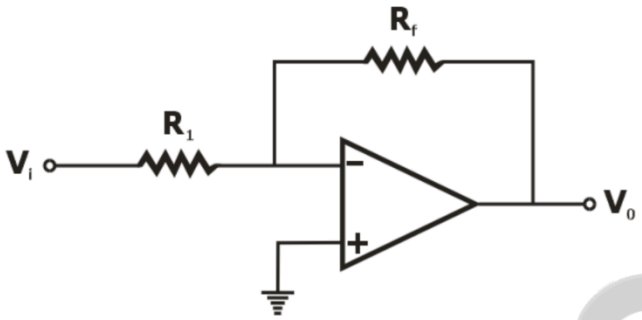


Figure: 1

2.2. Non-Inverting Amplifier:

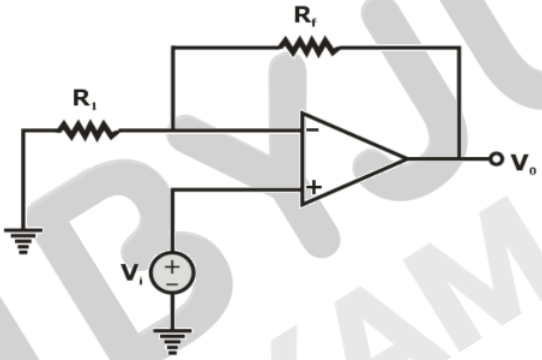


Figure 2: Non-Inverting Amplifier

$$A_V = \frac{V_0}{V_i} = 1 + \frac{R_f}{R_1}$$

2.3. Voltage Adder:

2.3.1. Inverting Adder:

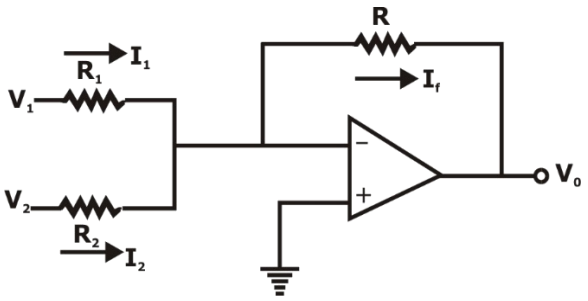


Figure: 3

$\therefore$ $\boxed{V_0 = -(V_1 + V_2)}$ if R1=R2=R

2.3.2. Non-Inverting Adder:

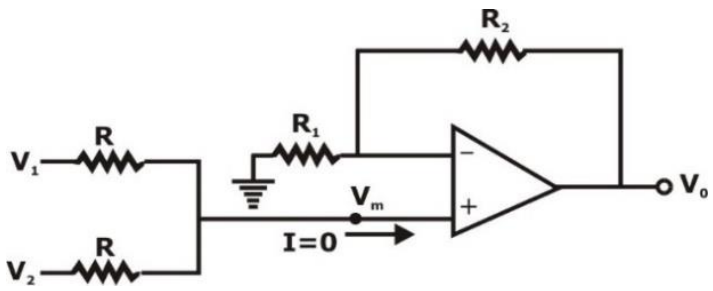


Figure: 4

$$\therefore \quad \boxed{V_0 = (V_1 + V_2)}$$

2.4. Voltage Subtractor Circuit

$$V_0 = \frac{R_f^{\,2}}{R_1 R_3} V_1 - \frac{R_f}{R_2} V_2$$

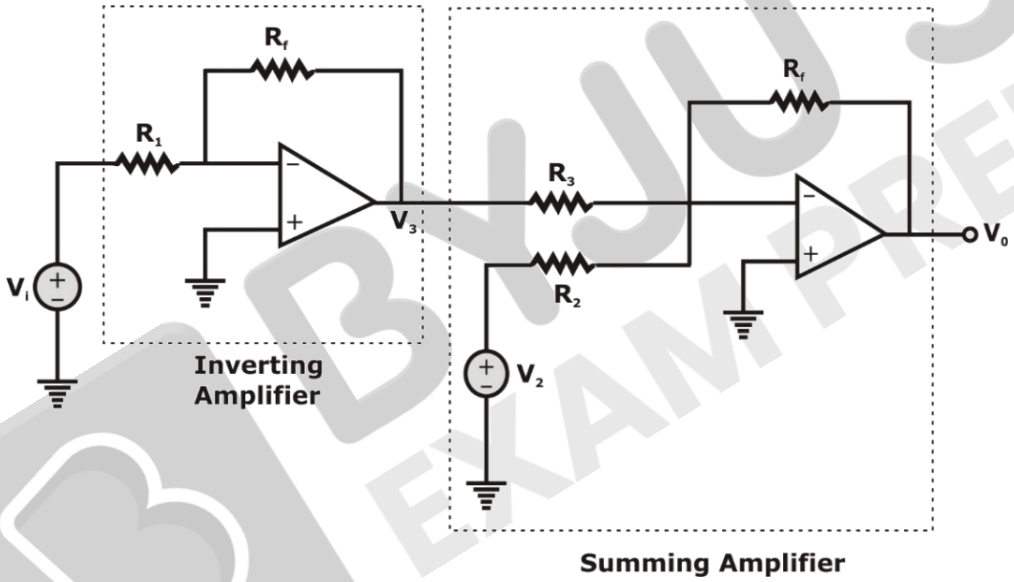


Figure 5: Voltage Subtractor Circuit

2.5. Differentiator circuit:

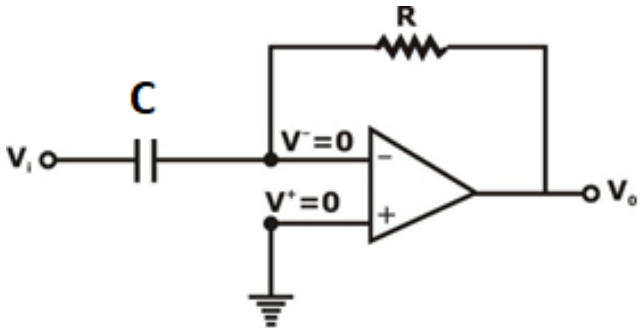


Figure 6: Differentiator circuit

$$V_0 = -RC\frac{dV_i}{dt}$$

2.6. Integrator circuit:

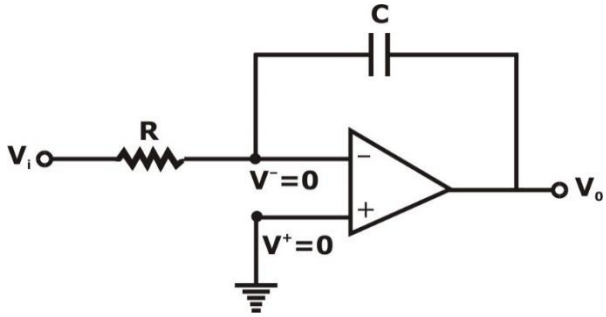
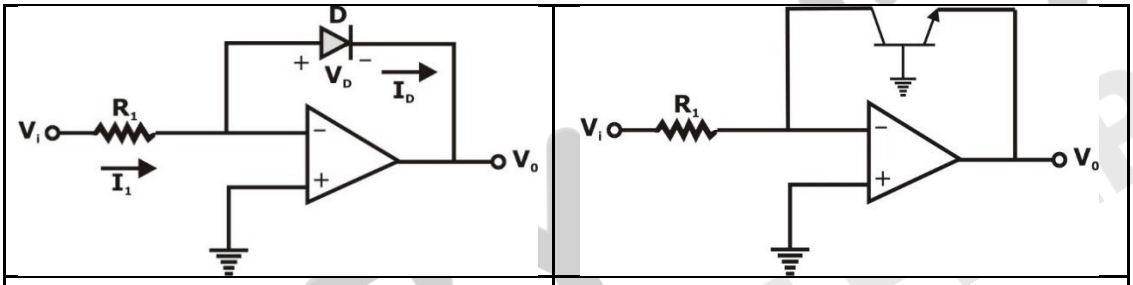


Figure 7: Integrator circuit

$$V_0 = \frac{-1}{RC}\int V_i dt$$

2.7. Logarithmic Amplifier:



Logarithmic Amplifier by using diode	Logarithmic Amplifier by using transistor

Figure: 8

$$V_0 = -V_T \ln\left[\frac{V_i}{I_S R}\right]$$

2.8. Exponential Amplifier:

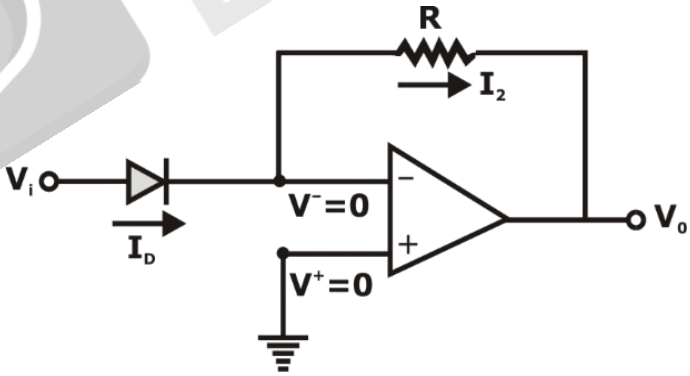


Figure 9: Exponential Amplifier

$$V_0 = -I_S R e^{V_i/V_T}$$

2.9. Square root amplifier:

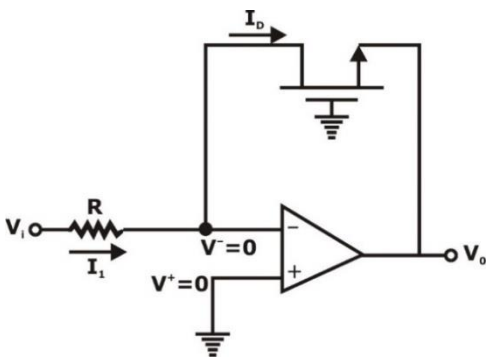


Figure: 10

$$V_0 = -\sqrt{\frac{2V_i}{\mu_n C_{ox}\frac{W}{L}R}} - V_T$$

2.10. Comparator: –

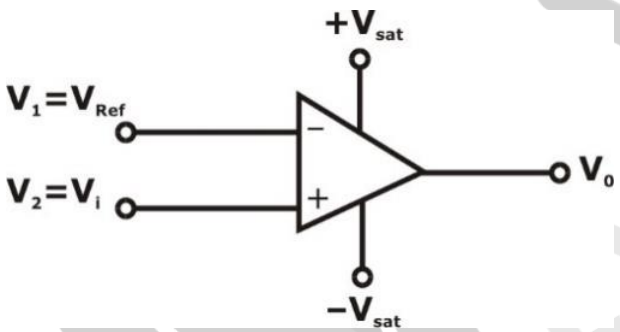
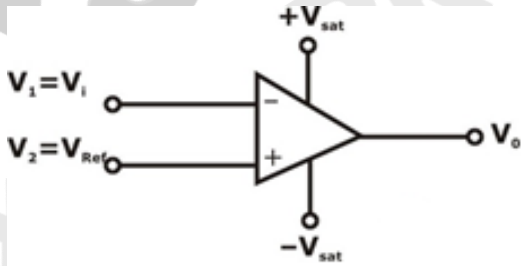
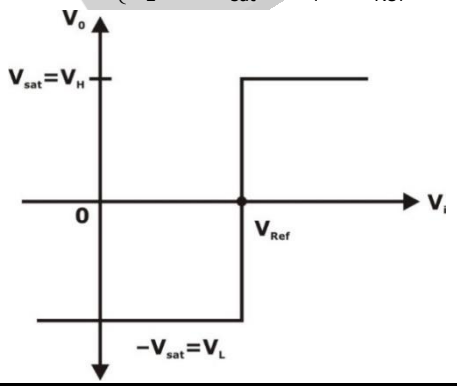
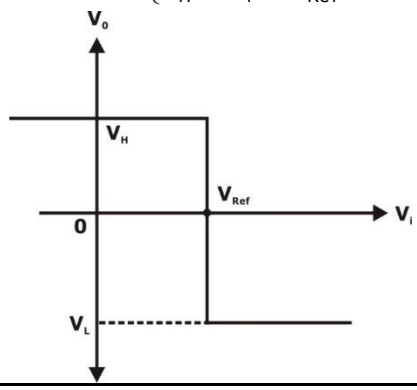
(a) Non-Inverting Comparator	(b) Inverting Comparator
	
$V_0 = \begin{cases} V_H = +V_{sat}, & V_i > V_{Ref} \\ V_L = -V_{sat}, & V_i < V_{Ref} \end{cases}$ 	$V_0 = \begin{cases} V_L, & V_i > V_{Ref} \\ V_H, & V_i < V_{Ref} \end{cases}$ 

Table 2: Comparator

2.11. Schmitt Trigger

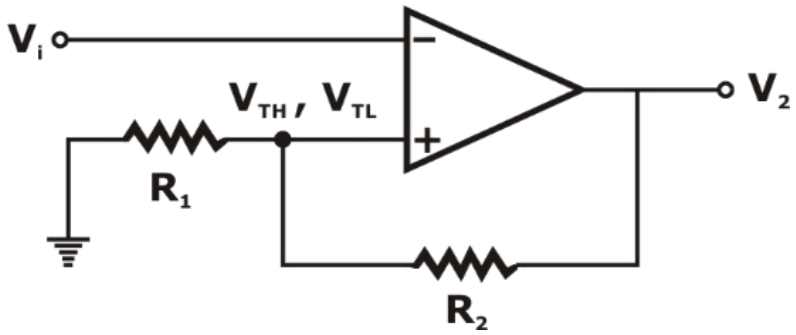


Figure 11: Basic Schmitt Trigger

2.11.1. Inverting Schmitt trigger:

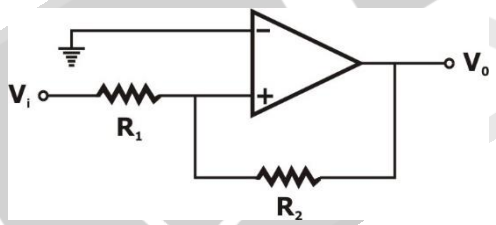
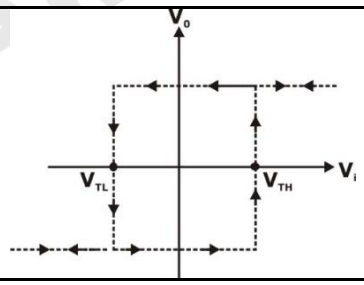
Here,

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right)V_H, \quad V_{TL} = \left(\frac{R_1}{R_1 + R_2}\right)V_L$$

2.11.1. Non Inverting Schmitt trigger:

$$V_{TH} = -\left(\frac{R_1}{R_2}\right)V_L$$

$$V_{TL} = -\left(\frac{R_1}{R_2}\right)V_H$$

	
Non-Inverting Schmitt trigger	**Voltage-Transfer Characteristics**

2.12. Precision Rectifier

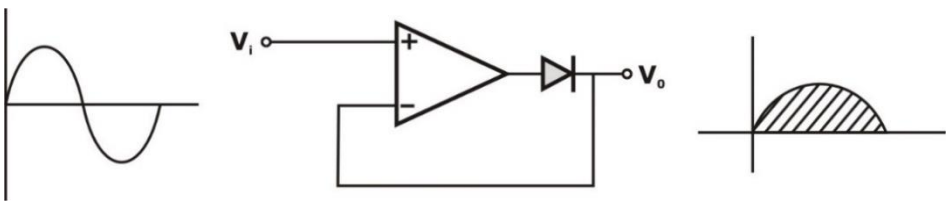


Figure 13:

2.13. Instrumentation Amplifier:

It consists of two non-inverting amplifiers and one difference amplifier.

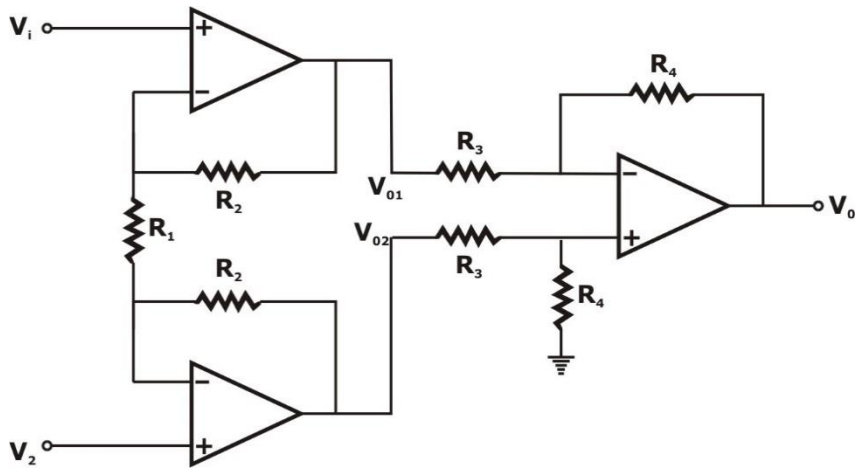


Figure 14: Instrumentation Amplifier

$$V_0 = \frac{R_4}{R_3}\left[1 + \frac{2R_2}{R_1}\right]\left[V_2 - V_1\right]$$

2.14. Astable Multivibrator:

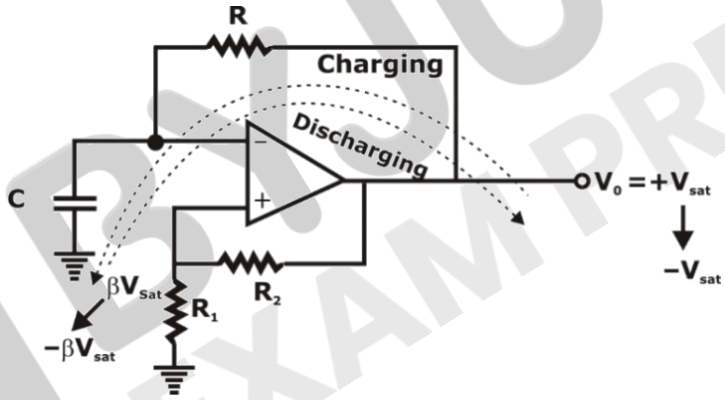


Figure 15: Astable Multivibrator

Here $\beta = \frac{R_2}{R_1 + R_2}$ = feedback fraction

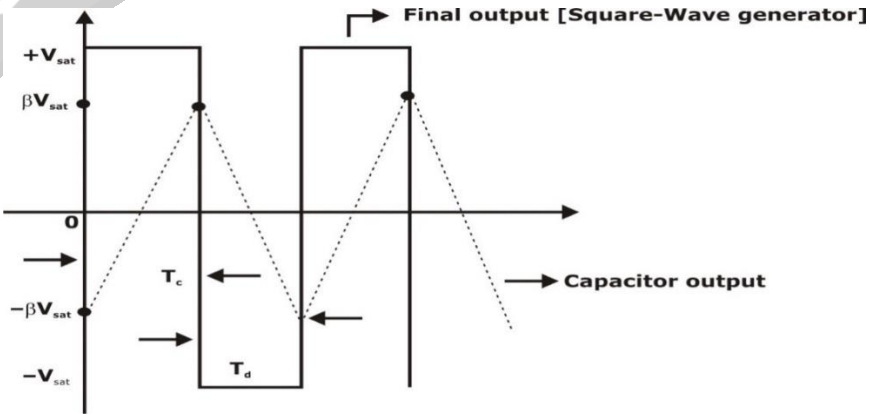


Figure 16: Waveform

Here,

T_C = charging time

T_d = discharging time

$$T_d = RC\ln\left[\frac{1+\beta}{1-\beta}\right]$$ Discharging time

$$T_C = RC\ln\left[\frac{1+\beta}{1-\beta}\right]$$ Charging time

$$T = T_d + T_C = 2RC\ln\left[\frac{1+\beta}{1-\beta}\right]$$ Total time period

Here, $\beta = \frac{R_2}{R_1 + R_2}$

$$f = \frac{1}{2RC\ln\left[\frac{1+\beta}{1-\beta}\right]}$$ Frequency of square wave generator

2.15. Bistable Multivibrator

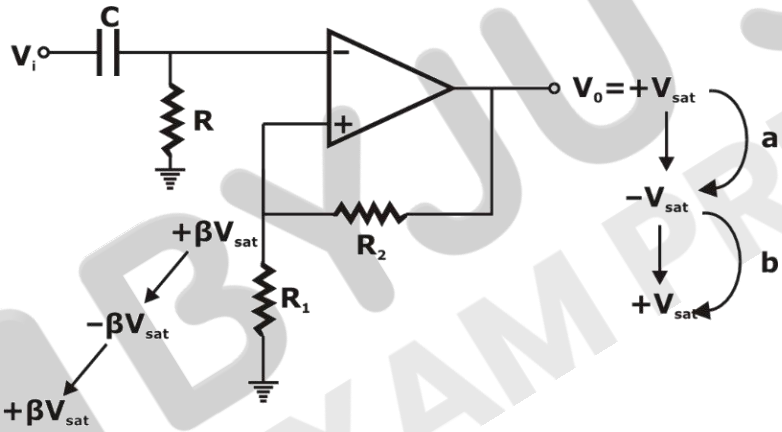


Figure 17: Bistable Multivibrator

Here, a to b changes only after triggering and before triggering, it will be constant = $+V_{sat}$

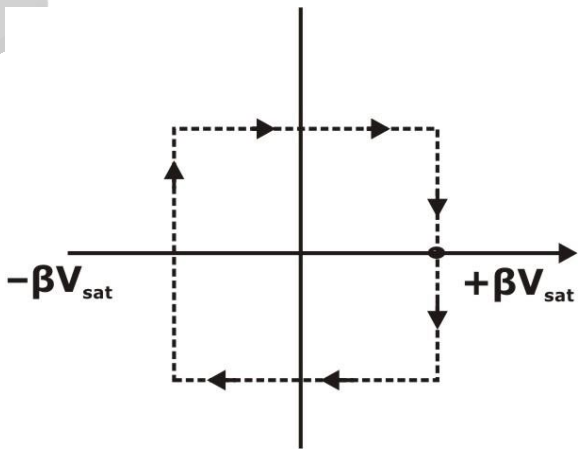


Figure:18

2.16. Monostable Multivibrator

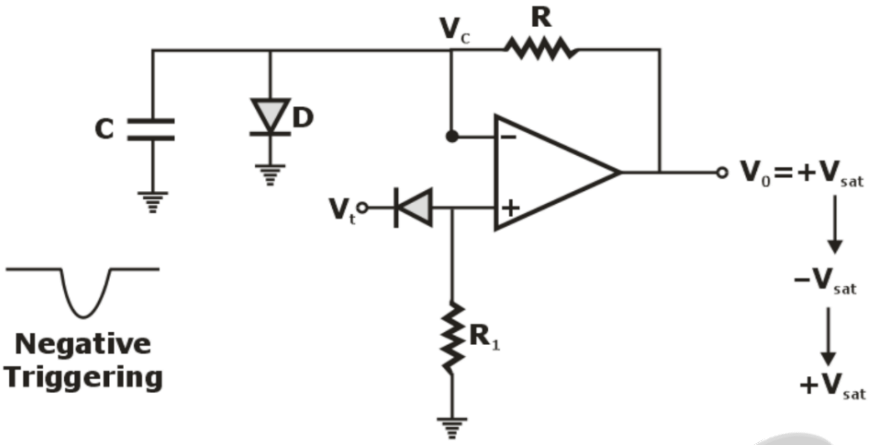


Figure 19: Monostable Multivibrator

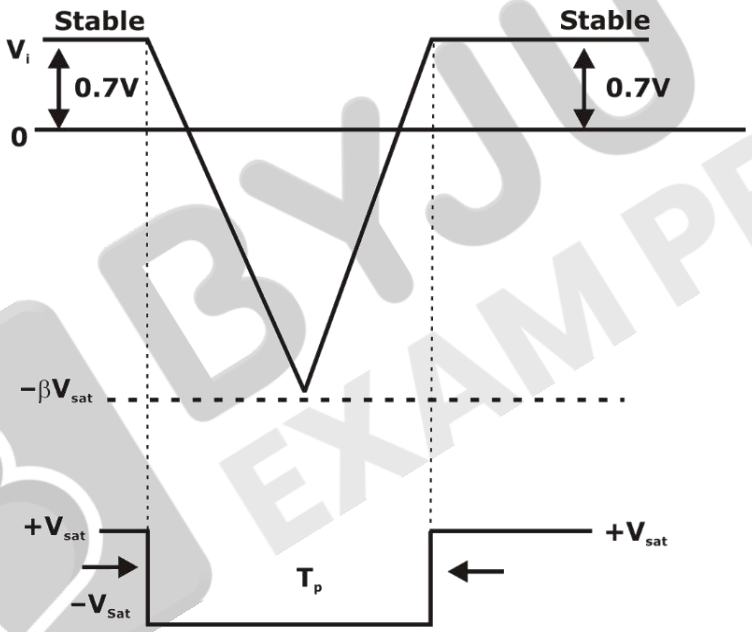


Figure:20 Waveform

Time Period of Monostable Multivibrator:

T_P=0.693RC

Other names of Monostable Multivibrator:

- One Shot Multivibrator
- Pulse Stretcher

CHAPTER 12 : OSCILLATORS

1. OSCILLATION CRITERION

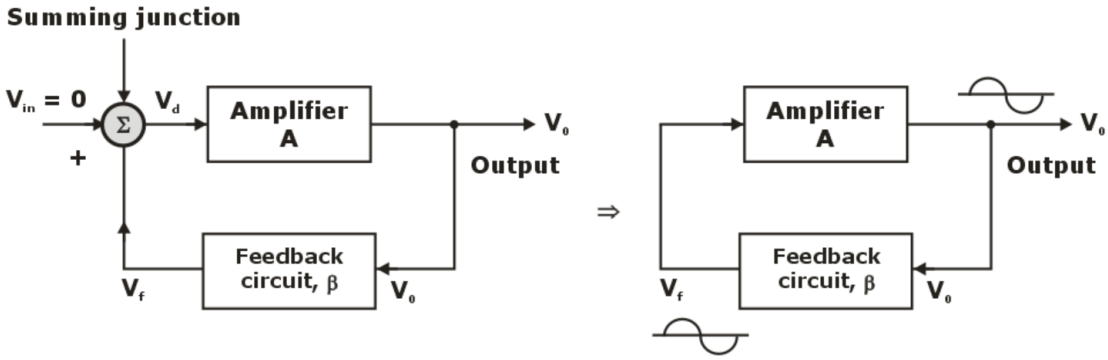


Figure 1: Oscillator Block Diagram

$$\frac{V_0}{V_{in}} = \frac{A}{1 - A\beta}$$

$$\boxed{A\beta = 1} \quad \text{.....} \quad \text{(i)}$$

Expressed in polar form $\boxed{A\beta = 1\angle 0^\circ \text{ or } 360^\circ}$ ..... (ii)

Equation (i) & (ii) gives two requirements for oscillation:

- The magnitude of the loop gain Aβ must be at least 1, and
- The total phase shift of the loop gain Aβ must be equal to 0° or 360°.

The above conditions is known as **Barkhausen** criterion.

2.OSCILLATOR TYPES:

Types of components used	Frequency of oscillation	Types of waveform generated
RC oscillator LC oscillator Crystal oscillator	Audio frequency (AF) Radio frequency (RF)	Sinusoidal Square wave Triangular wave Sawtooth wave etc.

Table 1

3. THE PHASE-SHIFT OSCILLATOR

3.1. Phase Shift Oscillator Using FET

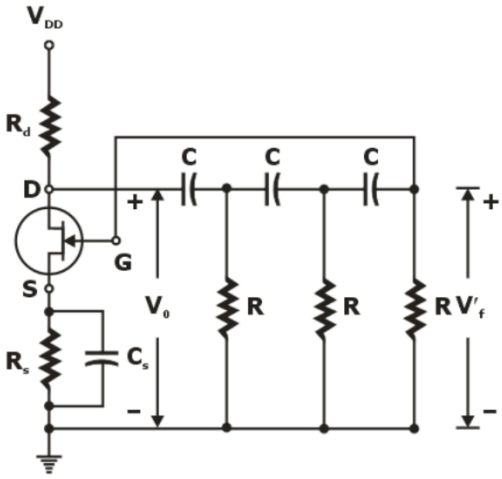


Figure 2(a): An FET Phase Shift Oscillator

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

At the frequency of oscillation,

$$\boxed{\beta = +\frac{1}{29}}$$

In order that |βA| shall not be less than unity, it is required that |A| be at least 29. Hence and FET with μ < 29 cannot be made to oscillate in such a circuit.

3.2. Phase Shift Oscillator Using BJT:

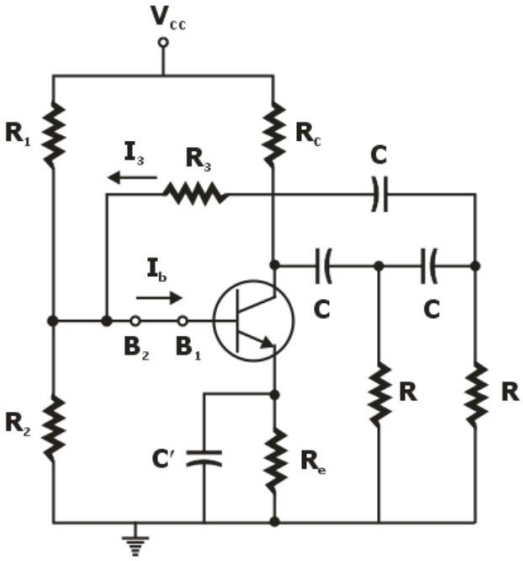


Figure 2(b): A Transistor Phase shift oscillator

The frequency of oscillation is given by

$$f = \frac{1}{2\pi RC} \cdot \frac{1}{\sqrt{6 + 4K}}$$

Where, K = R_C/R. The condition for sustaining of oscillation is given by

$$h_{fe} > 4K + 23 + \frac{29}{K}$$

3.3. Phase-Shift Oscillator with Op-Amp

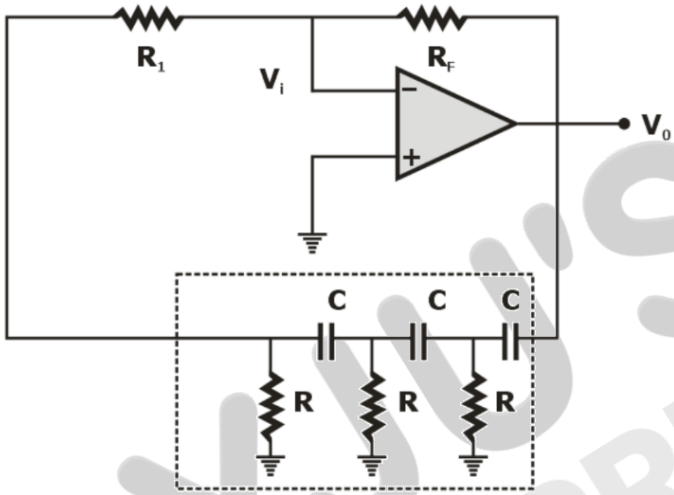


Figure 2(c): A Phase Shift Oscillator Using Op-amp

$$f_0 = \frac{1}{2\pi\sqrt{6}RC} = \frac{0.065}{RC}$$

At this frequency, the gain A must be at least 29.

That is,

$$\left|\frac{R_F}{R_1}\right| = 29 \qquad \text{or} \qquad R_F = 29R_1$$

3.4.Disadvantage:

The disadvantage of RC phase-shift oscillator is that the frequency of oscillation cannot be altered. In further we will study the oscillators in which frequency can be altered by changing circuit parameters.

4.WEIN BRIDGE OSCILLATOR:

$$f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

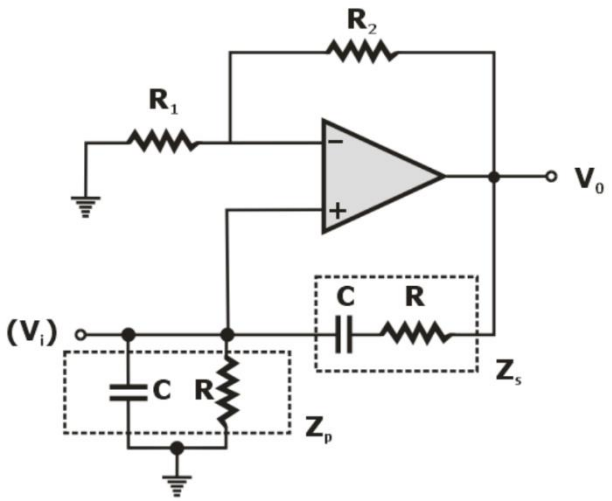


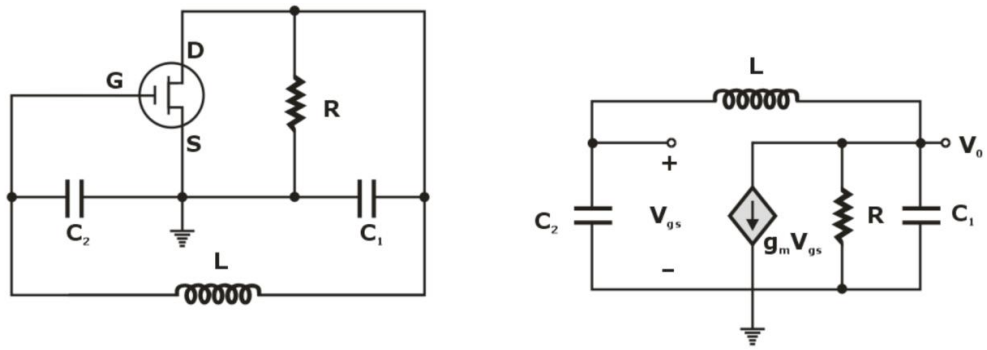
Figure 3: Wein- Bridge Oscillator

At this frequency the gain required for sustained oscillation is given by

$$A = \frac{1}{\beta} = 3$$

That is $1 + \frac{R_2}{R_1} = 3$ ➔ $\boxed{R_2 = 2R_1}$

5.1.COLPITTS OSCILLATOR:



(a) (b)

Figure 4: MOSFET Colpitts Oscillator (a) The ac equivalent circuit, (b) Small- Signal equivalent Circuit

$$\boxed{\omega_0 = \frac{1}{\sqrt{L\left(\frac{C_1C_2}{C_1 + C_2}\right)}}} \qquad \text{(i)}$$

From the real part, the condition for oscillation is

$$\frac{\omega_0^2 LC_2}{R} = g_m + \frac{1}{R} \qquad \text{(ii)}$$

combining equations (iii) and (iv) yields,

$$\boxed{\frac{C_2}{C_1} = g_m R} \qquad \text{(iii)}$$

where g_mR is the magnitude of the gain, Equation (v) states that to initiate oscillations spontaneously, it must have $g_mR > (C_2/C_1)$.

5.2. Colpitts Oscillator using BJT

Frequency of oscillation

$$f = \frac{1}{2\pi\sqrt{L\left(\frac{C_1C_2}{C_1 + C_2}\right)}} \quad \text{and} \quad \boxed{g_mR_C \geq \frac{C_2}{C_1}}$$

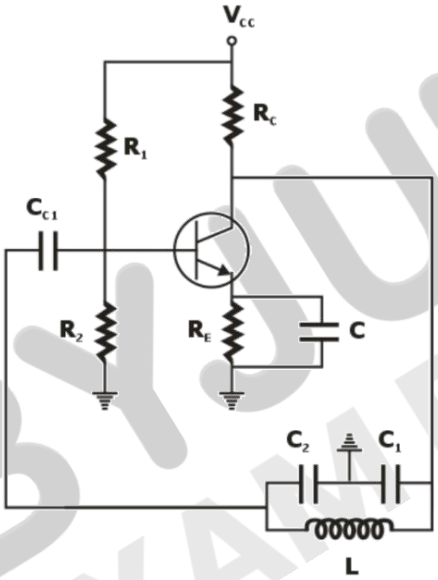


Figure 4(c): Colpitts Oscillator using BJT.

6. HARTLEY OSCILLATOR:

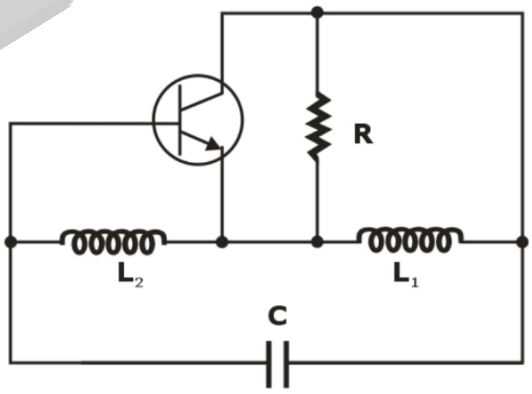


Figure 5: The ac equivalent BJT Hartley Oscillator

$$\boxed{\omega_0 = \frac{1}{\sqrt{(L_1 + L_2)C}}} \quad \text{and} \quad r_\pi \gg 1/\omega C_2.$$

7. CLAPP OSCILLATOR:

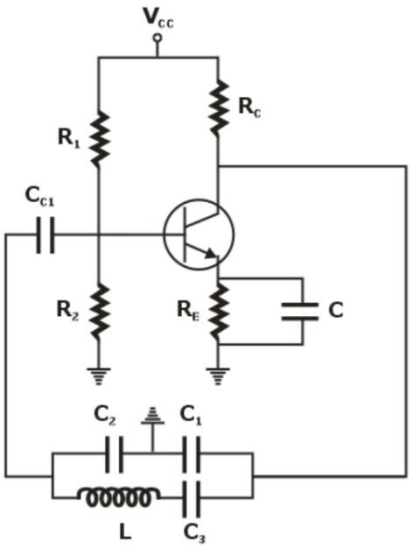


Figure 6: Clapp Oscillators

Frequency of oscillation

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}\right)}$$

If C_3 is selected such that it is much smaller than C_1' and C_2' then

$$\frac{1}{C_3} >> \frac{1}{C_1}+\frac{1}{C_2}$$

Thus,

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{L}\times\frac{1}{C_3}}$$

f_0 becomes independent of C_1 and C_2.

8.CRYSTAL OSCILLATORS

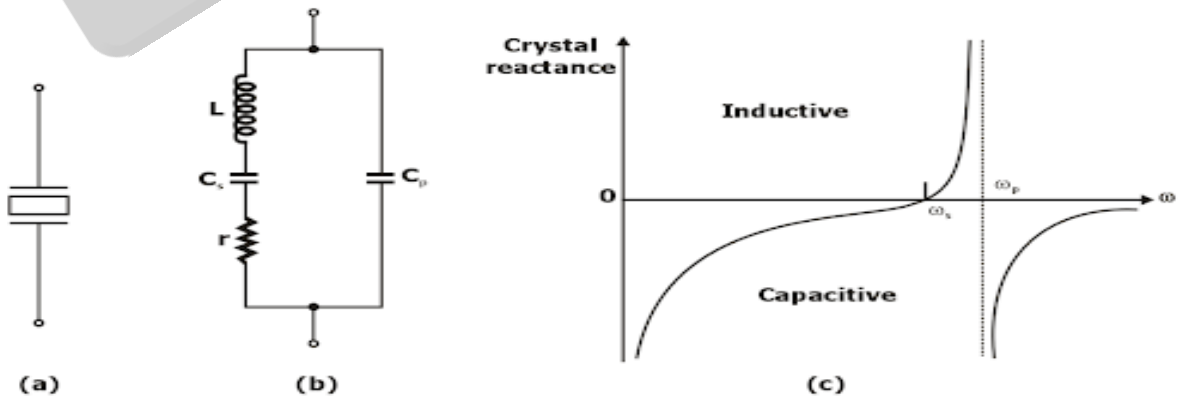


Figure 7: (a) Circuit Symbol, (b) Equivalent Circuit,
(c) Crystal reactance versus frequency

a series resonance at ω_s $\boxed{\omega_s = \frac{1}{\sqrt{LC_s}}}$

and a parallel at ω_p $\boxed{\omega_p = \frac{1}{\sqrt{L\left(\frac{C_s C_p}{C_s + C_p}\right)}}}$

$$\omega_0 \simeq \frac{1}{\sqrt{LC_s}} = \omega_s$$

S.No	Oscillator	Range of Frequency
1.	Phase shift	1Hz to 10MHz
2.	Wein-bridge	1Hz to 1MHz
3.	Colpitts	10kHz to 100MHz
4.	Hartley	10kHz to 100MHz
5.	Crystal	For fixed frequency
6.	Clapp	10kHz to 100MHz
7.	Negative resistance	>100mHz

Table 2

CHAPTER 13 : 555 TIMER & WAVE GENERATORS

1. THE 555 TIMER CIRCUIT

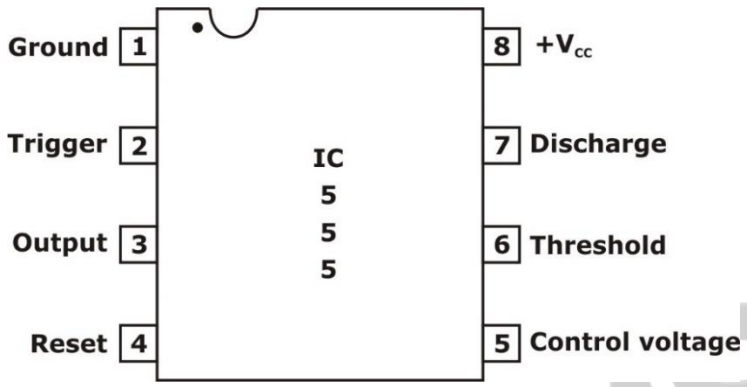


Figure 1(a): Pin diagram of 555 Timer

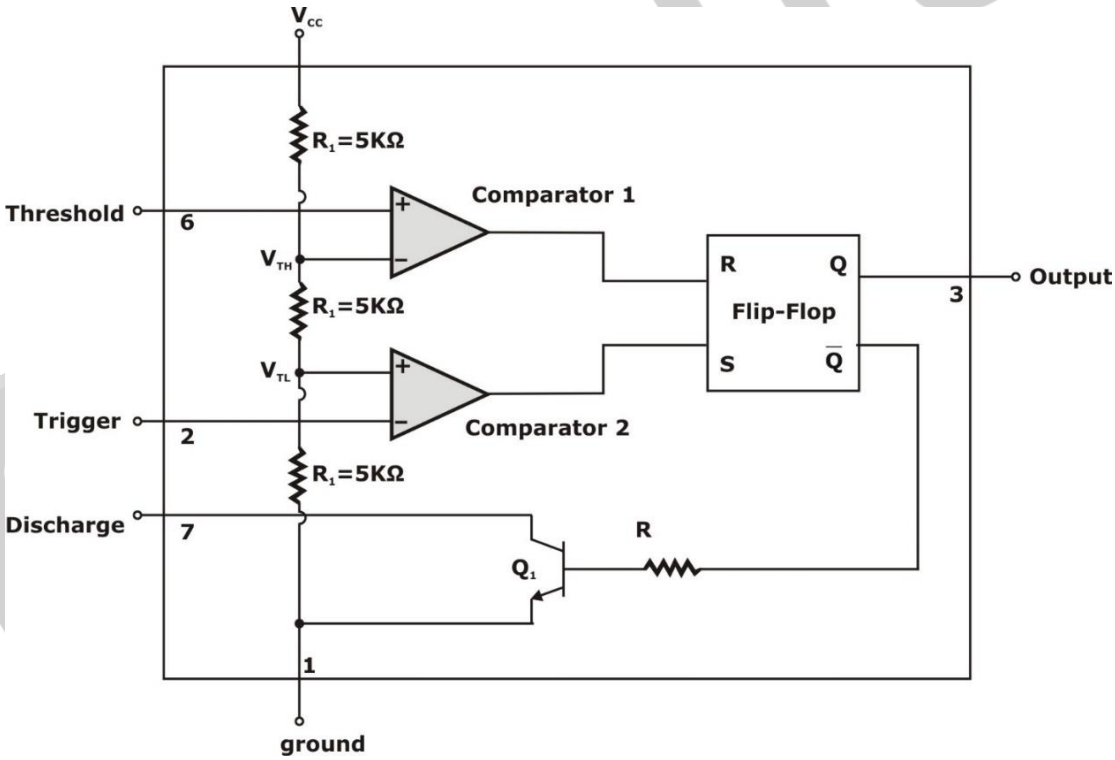


Figure 1(b): Block diagram representation of the internal circuit of the 555-IC timer.

$$V_{TH} = \frac{2}{3}V_{CC} \text{ for comparator 1}$$

And $$V_{TL} = \frac{1}{3}V_{CC} \text{ for comparator 2}$$

2. IMPLEMENTATION OF A MONOSTABLE MULTIVIBRATOR USING 555 TIMER

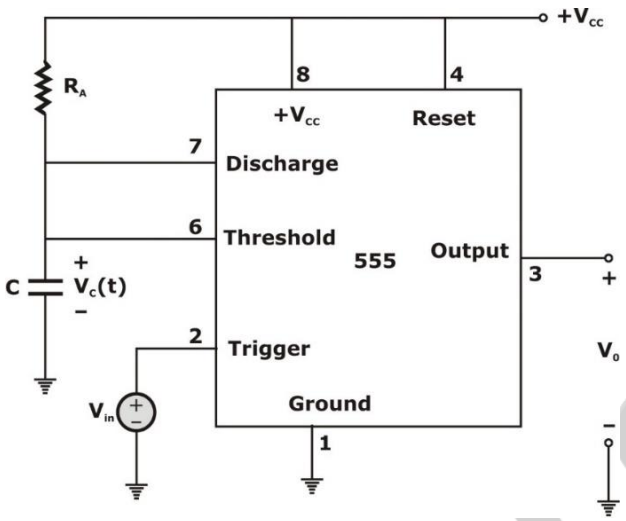


Figure 2(a): The 555 circuit connected as a monostable multi-vibrator.

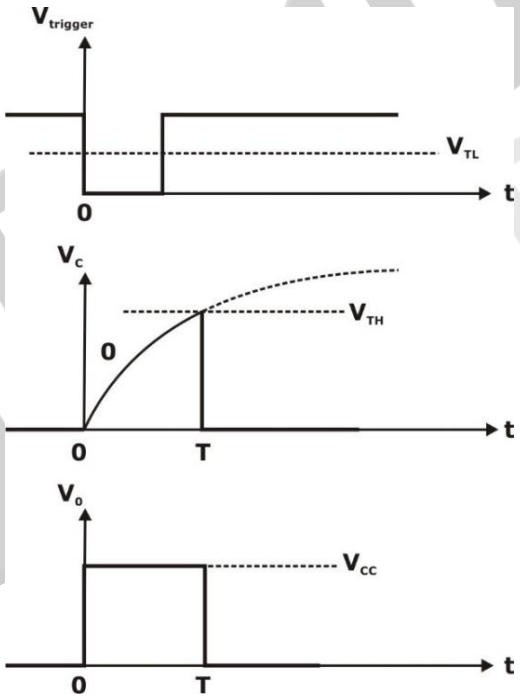


Figure 2(b): Waveform of circuit 2(a)

$\boxed{T=RC \ln(3)=1.1RC}$

3. IMPLEMENTATION OF ASTABLE MULTIVIBRATOR USING THE 555 TIMER

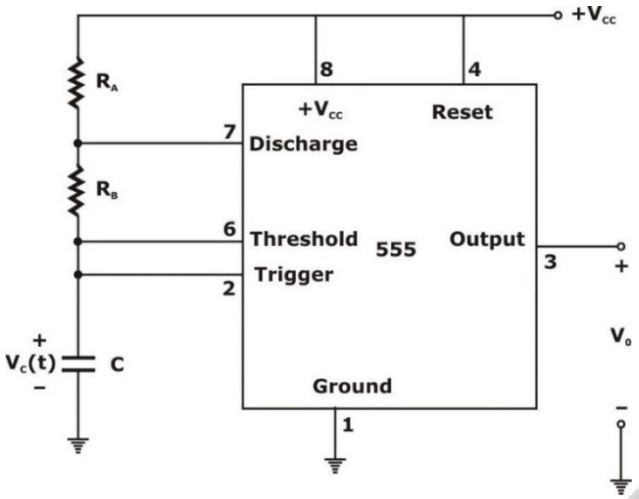


Figure 3(a): Astable Multivibrator 555 circuit.

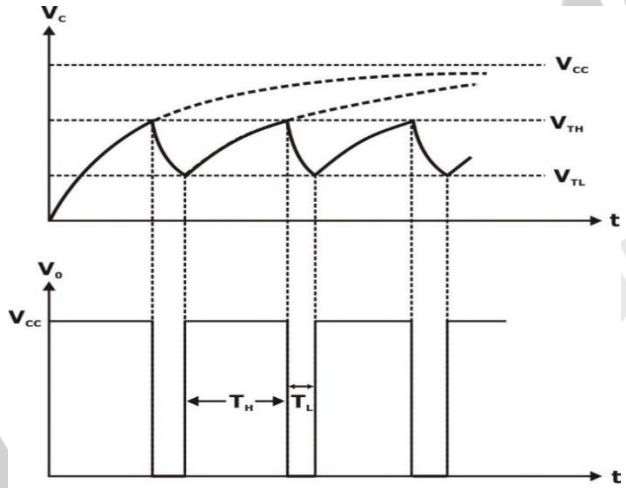


Figure 3(b): waveform of circuit 3(a)

$$\boxed{T_C = 0.693\,(R_A + R_B)C}$$

$$\boxed{T_D = \tau_B \ln(2) = 0.693\,R_B C}$$

$$\boxed{T = 0.693\,(R_A + 2R_B)C}$$

The frequency of oscillation,

$$f = \frac{1}{T} = \frac{1}{T_C + T_D}$$

$$\boxed{f = \frac{1}{0.693(R_A + 2R_B)C} = \frac{1.44}{(R_A + 2R_B)C}}$$

Duty cycle:

$$\boxed{\text{Duty cycle} = \frac{T_C}{T} \times 100\% = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%}$$

Duty cycle of the circuit is always greater than 50%.

****