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Rajasthan RVUNL

Electrical Engineering

Microprocessor and Microcontroller

Top 50 Most Important Questions

1. The instruction PCHL, in 8085 is used for

   A. Load PC with contents of HL.

   B. Load HL with contents of memory location pointed by PC.

   C. Load HL with content of PC

   D. Load PC with the contents of memory location pointed by HL pair.

Ans. A

Sol.: PCHL: (Loas program counter with HL contents) the content of registers H and L are copied into the [program counter. The contents of h are placed as a high-order and of L as a low order byte.

2. In 8 bit microprocessor, the high order register is:

   A. Flag register B. Accumulator

   C. Program Counter D. Stack pointer

Ans. B

Sol.: Option (b) is correct as Accumulator can hold data upto 8-bit and proceeds data by performing arithmetic and logic operations, where as other three options are of low order registers.

3. The DAD H instruction is performed in 8085 microprocessor, is similar to

   A. Shifting each bit one position left

   B. Shifting each bit one position right

   C. Shifting each bit position by 1 to left with zero inserted to LSB

   D. Shifting each bit position to right by 1 and inserting zero to MSB.

Ans. C

Sol.: The DAD H instruction is performed in 8085 microprocessorShifting each bit position by 1 to left with zero inserted to LSB. In this instruction HL register pair works as Accumulator. Because the 16-bit content of rp will be added with HL register pair(rp) content and sum thus produced will be stored back on to HL again.

Though it is an arithmetic instruction, by design, flags other than Cy, will not get affected by the execution of this instruction **DAD rp**.

4. CONSIDER the microprocessor 8085, choose which one of the following is incorrect information about these microprocessor

   A. In 8085 Flag is called as High order and Accumulator Low order Register

   B. LIFO (Last In First Out) stack is used in 8085

   C. Accumulator register, Temporary register, Instruction register, Stack Pointer, Program Counter are the various registers in 8085

   D. 5 Mhz is the Maximum clock frequency in 8085.

Ans. D

Sol.: 5 Mhz is the Maximum clock frequency in 8086 microprocessor.

5. In 8085, TRAP is

A. always maskable

B. cannot interrupt a service sub-routine

C. used for catastrophic events like temporary power failure

D. lowest priority interrupt

Ans. C

Sol.: In 8085, TRAP is used for catastrophic events like temporary power failure.

6. The 8085 instruction that doubles the value in accumulator is

A. XRA A

B. ADD A

C. SUB A

D. ORA A

Ans. B

Sol.: ADD A instruction add the contents of accumulator with the contents of accumulator itself, resulting in double the value of the accumulator.

7. Which of the following is not a valid arithmetic instruction in 8085?

A. SBI

B. SUI

C. AXI

D. LXI

Ans. C

Sol.: AXI is not a valid arithmetic instruction in 8085.

SBI: Subtract immediately from the content of the accumulator and the result is stored in the accumulator.

SUI: - Subtract immediate from accumulator. This instruction subtract the immediate data from the content of the accumulator and the result is stored in the accumulator.

8. Call instruction when executed by 8085 microprocessor needs

A. 16 T-states

B. 14 T-states

C. 18 T-states

D. 12 T-states

Ans. C

Sol.: CALL instruction has 5 machine cycles and 18 T-states

One opcode fetch cycle → 6 T-states

Two memory read cycles → 6 T-states

Two memory write cycles → 6 T-states

9. Number of possible pages in 8085 microprocessor is-

A. 64

B. 128

C. 256

D. None of these

Ans. C

Sol.: In 8085 total memory size is 64 KB and each page has 256 bytes.

So, total number of possible pages = $\frac{64KB}{256 \times 8}$ = 256 Pages

10. An n-bit microprocessor has

A. n-bit program counter
B. n-bit address register
C. n-bit ALU
D. n-bit instruction registers

Ans. D

Sol.: In computer architecture, 32-bit integers, memory addresses, or other data units are those that are 32 bits (4 octets or 4 Bytes) wide. 32-bit microcomputers are computers in which 32-bit microprocessors are the norm. We know that n-bit microprocessor can handle n-bit instruction size/registers.

11. The addressing mode for the instruction "RET" is

A. Register addressing mode
B. Immediate addressing mode
C. indirect addressing mode
D. Direct addressing mode

Ans. C

Sol.:

12. An 8085 assembly language program is given as follows.

LXI H, 8100 H
MVI M, 20 H
MVI A, 40 H
INX H
MVI M, 30 H
ADD M
HLT

The value of A at the end of the execution of the program is

A. 90 H
B. 0 H
C. 40 H
D. 60 H

Ans. B

Sol.: HL 8100 H

M ← 20 H

A ← 40 H

M ← 30 H

A ← A + M

A ← $(30)_H + (40)_H$

A ← $(70)_H$

13. What is content of accumulator of 8085 μ_P after the execution of XRI F0 H instruction?

A. Only the upper nibble of accumulator is complemented
B. Only the lower nibble is complemented
C. Only the upper nibble ie reset to zero.
D. Only the lower nibble ie reset to zero.

Ans. A

Sol.: Data in accumulator 00H

```
        0 0 0 0     0 0 0 0 ⟶ 0 0
EX-OR
        1 1 1 1     0 0 0 0 ⟶ 0 0
        ---------------------------
        1 1 1 1     0 0 0 0 ⟶ Store in accumulator
```

i.e. only upper nibble of accumulator is complemented.

14. In an Intel 8085 A, what is the content of the Instruction Register (IR)?

A. Op-code for the instruction being executed

B. operand for the instruction being executed

C. Op-code for the instruction to be executed next.

D. Operand for the instruction to be executed next.

Ans. A

Sol.: IR contains the opcode for the instruction being executed while PC contains address of next instruction to be executed.

15. How many general purpose registers in 8085 microprocessor?

A. 3

B. 5

C. 6

D. 7

E. None of these

Ans. C

Sol.: The 8085 microprocessor has **6 general purpose** registers to store 8 bit data. These are B, C, D, E, H, L . They can be combined as registers pair **BC, DE** and **HL** to perform 16 bit operations.

16. For the 8085 assembly language program given below, the content of the accumulator after the execution of the program is

```
3000  MVI  A,  45H
3002  MOV  B,  A
3003  STC
3004  CMC
3005  PAR
3006  XRA  B
```

A. 00H

B. 45H

C. 67H

D. E7H

Ans. C

Sol.: Instruction Content

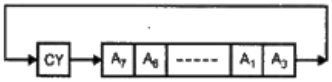
MVI A, 45H A = 45 H (= 01000101)

MOV B, A B = 45 H

STC CY = 1

CMC CY = 0

RAR



A = 00100010

XRA B A ← (00100010) (c) (01000101)

or A ← 01100111

or A ←67 H

Therefore, the content of the accumulator after the execution of the program is 67 H.

17. The following program starts at location 0100H

LXI SP,00FF

LXI H, 0701

MVI A,20H

SUB M

The content of accumulator when the program counter reaches 0107 H is

A. 20 H B. 02 H

C. 00 H D. FF H

Ans. C

18. Single instruction to clear the lower four bits of the accumulator in 8085 assembly language is

A. XRI0FH B. ANIF0H

C. SRIF0H D. ANIOFH

Ans. B

Sol.: To clear the lower 4-bits of an accumulator ANI FO H

$$A = a_7\ a_6\ a_5\ a_4\ a_3\ a_2\ a_1\ a_0$$
$$FOH = 1\ \ 1\ \ 1\ \ 1\ \ 0\ \ 0\ \ 0\ \ 0$$
$$ANI\quad a_7\ a_6\ a_5\ a_4\ \ 0\ \ 0\ \ 0\ \ 0$$

19. Which of the following is/are the functions of microprocessor?

A. If performs the logical and mathematical operations using its ALU.

B. It controls data flow in a system and hence can transfer data from one location another.

C. It takes necessary decision.

D. All of above

Ans. D

Sol.: A microprocessor performs the following functions:

(i) If performs the logical and mathematical operations using its ALU.

(ii) It controls data flow in a system and hence can transfer data from one location another.

(iii) It takes necessary decision.

20. If the HLT instruction is executed in INTEL 8085 then

A. the microprocessor enters into halt state and buses are tristated

B. the microprocessor is disconnected from the system bus till the reset is pressed.

C. the microprocessor halts the execution and load 0000 H to the program counter.

D. None of these

Ans. B

Sol.: The Halt will stop the processor from further execution; it can be restarted again only by an interrupt. A reset signal applied to the MP will abort the Halt. The MP may enter a Hold state, as the result of another device wanting the bus, from a Halt, but will return to the Halt state when the Hold is canceled.

21. For the 8085 assembly language program given below, the content of the accumulator after the execution of the program is

```
3000    MVI A,    45 H
3002    MOV B,    A
3003    STC
3004    CMC
3005    RAR
3006    XRA       B
3007    HLT
```

A. 00 H B. 45 H

C. 67 H D. E7 H

Ans. C

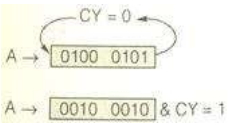
Sol.: MVI A, 45H // A ← 45H

MOV B, A // B ← A

STC // Set carry : CY = 1

CMC // Complement the carry i.e. CY = 0

RAR // Rotate accumulator right through carry



XRA B // Perform EX-OR operation with B and store in A

```
A→0010 0010
B→0100 0101
  0110 0111
```

A →67H

22. If the accumulator of an 8085 microprocessor is having 37H and form previous executions carry is already set to 1 . The accumulator contains what data after execution of ACI 56H.

A. 8DH
B. 8EH
C. 7EH
D. 84H

Ans. B

Sol.: ACI 56H results in: (A) + 56H + Cy

⇒ 56H + 37H + 01H = 8EH

23. The content of accumulator after the execution of following instructions will be

MVI A, B7 H

ORA A

RAL

A. 6E H
B. 6F H
C. EE H
D. EF H

Ans. A

Sol.: A = B7 H

ORA A: CY = 0, AC = 0

RAL: Rotate left with carry

A = 6E H

24. Write an instruction which takes the minimum possible time to clear the accumulator of the 8085.

A. ADD A,B
B. RST A
C. XOR A
D. SUB A,0

Ans. C

Sol.: XOR A

When this instruction is executed content of A becomes Zero (i.e. clear).

25. The Complement Accumulator (CMA) instruction of 8085 processor on execution affects

A. Zero Flag
B. Sign Flag
C. Carry Flag
D. None of the flags

Ans. D

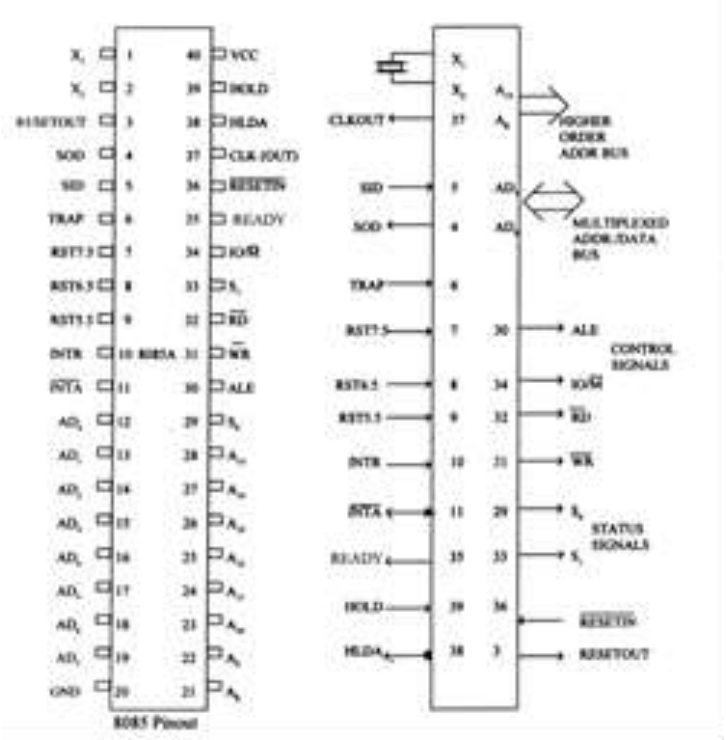
Sol.: CMA instruction does not affect any flag but it just complements the contents of the accumulator. Flags are affected when only arithmetic and logical operations are done in ALU. CMA is neither an arithmetic nor logical operation.

26. 8085 has how many number of pin?

A. 16
B. 20
C. 40
D. 32

Ans. C

Sol.:



27. An 8085 assembly language program is given below. Assume that the carry flag is initially unset. The content of the accumulator after the execution of the program is

```
MVI   A, 07H
RLC
MOV   B, A
RLC
RLC
ADD   B
RRC
```

A. 8C H

B. 64 H

C. 23 H

D. 15 H

Ans. C

Sol.: Carry flag = 0

MVI,A,07H : A = 0000 0111

Rotating left without carry A = 0000 1110

MOV B,A : A = B = 0000 1110

Rotating A = 00011100

Again rotating A = 0011 1000

Add B : A = 0100 0110

Rotating on to right A = 0010 011

A = 23H

Hence option C is correct

28. If in a microprocessor, there are 14 address lines and 8 data lines. The capacity of microprocessor will be:

A. 64Kb B. 128kB

C. 32kB D. 16kB

Ans. D

Sol.: Addressing capacity of the microprocessor can be calculate as:

$= 2^n \times$ m bits

Where, n is number of addressing lines

m is number of data lines = $2^{14} \times 8$ bits = $2^{10} \times 2^4$ bytes

Capacity = 16kB

29. In 8085 microprocessor which mode of addressing does the instruction CMP M use?

A. Direct addressing B. Register addressing

C. Indirect addressing D. Immediate addressing

Ans. C

Sol.: CMP M (Compare memory with accumulator)

The addressing mode is register indirect.

30. A microprocessor is ALU

A. and control unit on single chip

B. and memory on single chip

C. register unit and input output device on a single chip

D. register unit and control unit on single chip

Ans. D

Sol.: A µP is ALU + Register + CU on single chip manufactured by using VLSI technology.

31. In an instruction of 8085 microprocessor how many bytes are present?

A. One or two B. One, two or three

C. Only one D. Two or three

Ans. B

Sol.: CMC → one byte instruction

ADI 04H → two byte instruction

JMP 2030 → three byte instruction

32. Assume that the accumulator and the register C of 8085 microprocessor contain respectively F0 H and 0F H initially. What will be the content of accumulator after execution of instruction ADD C?

A. 00 H B. FF H

C. EF H D. FE H

Ans. B

Sol.: Accumulator → F 0H

Register → O FH

F FH

33. To multiply a number by 8 in 8085 we have to use RAL instruction:

A. Once B. Twice

C. Thrice D. Four times

Ans. C

Sol.: RAL is rotate accumulator left. Basically RAL operation is equivalent to multiplying by 2 every time. So when RAL instruction is executed, the accumulator is left shifted by one bit, and the value is added to itself for one time. So, basically we can write: $N= 2^n$, where 'N' is the number that is to be multiplied. So, here $2^3=8$. Answer is option (c)

34. In 8085 processor the HOLD and HLDA pin is used for ….

A. Memory Interfacing B. 8259 Interfacing

C. DMA Interfacing D. Co-processor Interfacing

Ans. C

Sol.: These two pins are used for DMA interfacing for direct transfer of data between I/O and Memory.

35. The 8085 microprocessor responds to the presence of an interrupt

A. As soon as the TRAP pin becomes 'LOW'

B. By checking the TRAP pin for 'high' status at the end of each instruction fetch

C. By checking the TRAP pin for 'high' status at the end of the execution of each instruction

D. By checking the TRAP pin for 'high' status at regular intervals

Ans. C

Sol.: TRAP is non-maskable interrupt and is active high level, edge triggered non-maskable highest priority interrupt.

36. If the CALL instruction of 8085 in the main program is conditional then RETURN instruction in the subroutine can be

A. Conditional

B. Conditional or unconditional

C. Can be determined by DDA instruction

D. Unconditional

Ans. B

Sol.: RETURN instruction can be conditional or unconditional in the subroutine.

37. If OR and XOR instruction is executed in 8085 microprocessor then which flags are fixed

A. AC, CY B. CY, P, AC

C. CY, S, Z D. All flags depend on result in accumulator.

Ans. A

Sol.: Auxiliary carry flag and carry flag is fixed to 0 in OR and XOR gate.

38. The 8085 Microprocessor has

A. 16-bit data bus 16-bit address bus B. 8-bit data bus 16-bit address bus

C. 16-bit data bus 8-bit address bus D. 8-bit data bus 8-bit address bus

Ans. B

Sol.: 8085 has 8 bit data bus and 16 bit address bus

39. Which instruction in an 8085 processor can set a flag?

A. MOV B, C B. JNZ 21 00 H

C. STA 20 00 H D. ADD B

Ans. D

Sol.: Rest are data transfer and control instructions.

40. Consider the following 8085 interrupts:

1). TRAP 2). INTR

3). RST 6 4). RST 7.5

5). RST 0

The software interrupts are

A. 1 and 3 only

B. 2 and 5 only

C. 3 and 5 only

D. 1, 2, 3, 4 and 5

Ans. C

Sol.: Microprocessor 8085 has 5 hardware interrupts which are:

TRAP, RST 7.5, RST 6.5

RST 5.5 INTR and rest interrupts are software interrupts.

So RST0 and RST6 are software interrupts.

41. Which one of the following is not an addressing Mode in 8085?

A. Immediate

B. Indirect

C. Register D. Segment

Ans. D

Sol.: Addressing modes in 8085 is classified into 5 groups.

1) Direct addressing mode

2) Register addressing

3) Immediate addressing

4) Implied Addressing

5) Immediate addressing

42. The content of the accumulator of 8085 microprocessor after execution of the following instructions will be

MVI A, A7h

ORA A

RLC

A. FFh B. 4Fh

C. 3Fh D. CEh

Ans. B

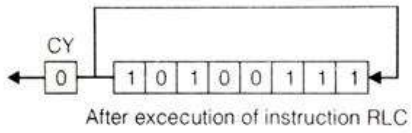
Sol.: *A* = 10100111 (*A7H*)

Logical OR with A

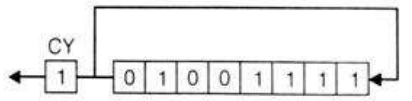
1010 0111

$\frac{1010\ \ 0111}{1010\ \ 0111}$, *CY* = 0

Before execution of instruction RLC



After excecution of instruction RLC



A = 4FH

43. For which one of the following, the instruction XRA A in 8085 microprocessor can be used?

A. Set the carry flag

B. Set the zero flag

C. Reset the carry flag and clear the accumulator

D. Transfer FFH to the accumulator

Ans. B

Sol.: ∵ $A \oplus A = 0$

∴ It is used to set the zero flag.

44. The addressing mode which makes use of in-direction pointers is _____

A. Indirect addressing mode

B. Index addressing mode

C. Relative addressing mode

D. Offset addressing mode

Ans. A

Sol.: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.

45. The crystal frequency of 8085 microprocessor is 6 MHz. The time required to execute instruction XTHL over this microprocessor.

A. 5.33 μsec B. 10.67 μsec

C. 4.33 μsec D. 8.67 μsec

Ans. A

Sol.: Microprocessor internally divides the crystal frequency by 2 with the help of filp- flop. Since, the crystal frequency is given as 6 MHz.

So, time period $= \frac{1}{3\times10^{6}\text{Hz}} = \frac{10^{-6}}{3}\text{sec}$

Since instruction XTHL consumes 16 T states to execute an instruction.

$$= \frac{16\times10^{-6}}{3} = 5.33\mu\text{sec}$$

46. In 8085, the DAA instruction is used for

A. Direct Address Accumulator B. Double Add Accumulator

C. Decimal Adjust Accumulator D. Direct Access Accumulator

Ans. C

Sol.: DAA → stand for decimal adjust accumulator, it is used for BCD additions.

47. Find the content of the accumulator after the execution of the following program:

MVI A, FO H

ORI FFH

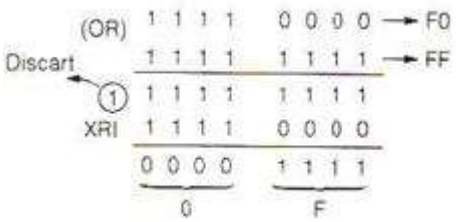
XRI FOH

A. 00 H B. F0 H

C. OF H D. FF H

Ans. C

Sol.:



Hence the content of accumulator will be 0F H.

48. In 8085 A microprocessor, the operation performed by the instruction **LHLD 2100$_H$** is

A. (H)←21H,(L)←00HH←21H, L← 00H

B. (H)←M(2100H),(L)←M(2101H)H←M2100H, L←M2101H

C. (H)←M(2101H),(L)←M(2100H)H←M2101H, L←M2100H

D. (H)←00H,(L)←21HH←00H, L←21H

Ans. C

Sol.: Instruction given is:

LHLD 2100H

The operation performed by this instruction is load HL register pair from the specified address in the instruction, directly. HL register pair is required 2-Byte data, but in 8085 at one address it contains only one-byte data, so this instruction will access two memory locations.

So, first byte address (i.e., 2100H) is mentioned in instruction itself and by default second-byte data is accessed from the next location (i.e., 2101H). Lower address data will be copied to lower byte [i.e., (L)←M(2101H)] and higher address data will be copied to higher byte [i.e, (H)←M(2101H)]

49. XCHG instruction of 8085 exchanges the content of

A. top of stack with contents of register pair

B. BC and DE register pair

C. HL and DE register pairs

D. None of the above

Ans. C

50. For differentiating I/O and memory operation, which pin no is used in 8085 microprocessor.

A. 32 B. 31

C. 34 D. 33

Ans. C

Sol.: Pin no. — 34 (IO/$\bar{M}$)

For IO it is set high and for memory operations it is low.

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