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Rajasthan RVUNL

Electrical Engineering

Microprocessor and Microcontroller

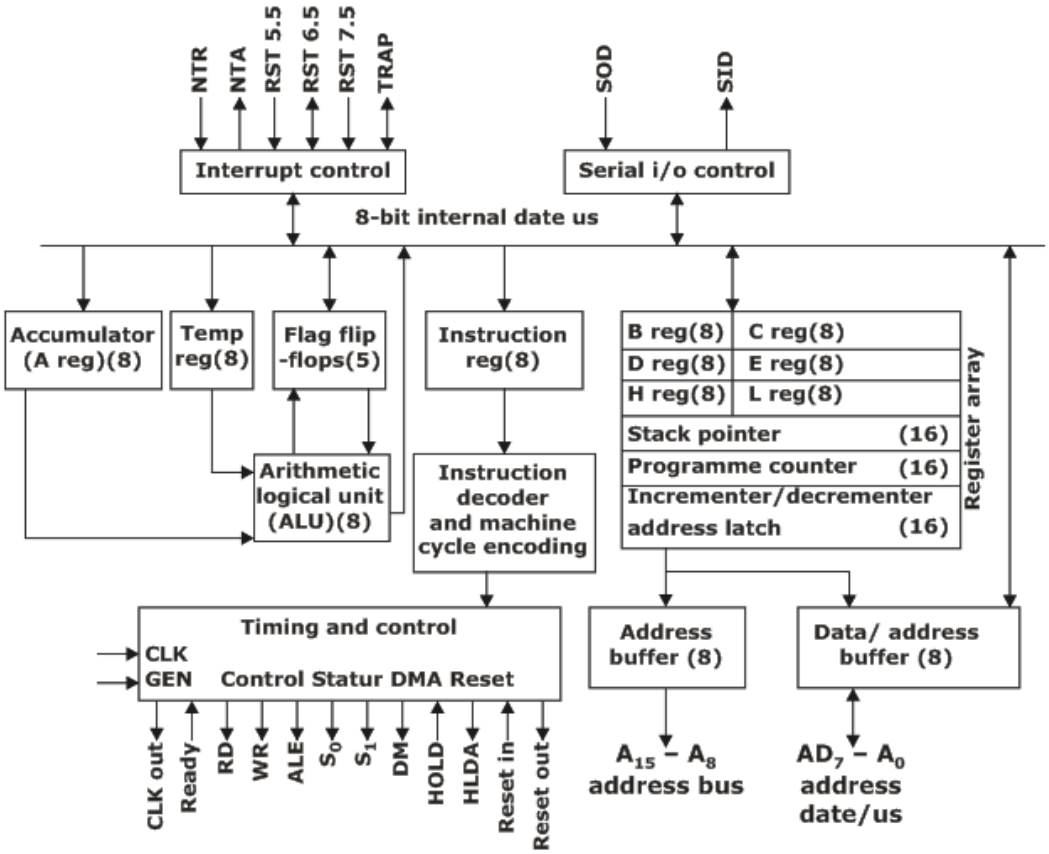
100 Days Important Formula Notes

MICROPROCESSOR & MICROCONTROLLER (FORMULA NOTES)

Microprocessor: A microprocessor includes ALU, register arrays and control circuits on a single chip.

Microcontroller: A device that includes microprocessor, memory and input and output signal lines on a single chip, fabricated using VLSI technology.

Architecture of 8085 Microprocessor



8085 MPU:

- 8 bit general – purpose microprocessor capable of addressing 64 K of memory.
- It has 40 pins, requires +5V single power supply and can operate with 3 – MHz single phase clock.

Accumulator: Is an 8 bit register that is used to perform arithmetic and logic functions.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z		AC		P		CY

Carry Flag (CY): If an arithmetic operation result in a carry or borrow, the CY flag is set, otherwise it is reset.

Parity Flag (P):

If the result has au even number of 1s, the flag is set, otherwise the flag is reset.

Auxiliary Carry (AC): In an arithmetic operation

- If carry is generated by D_3 and passed to D_4 flag is set.
- Otherwise, it is reset.

Zero Flag (Z): Zero Flag is set to 1, when the result is zero otherwise it is reset.

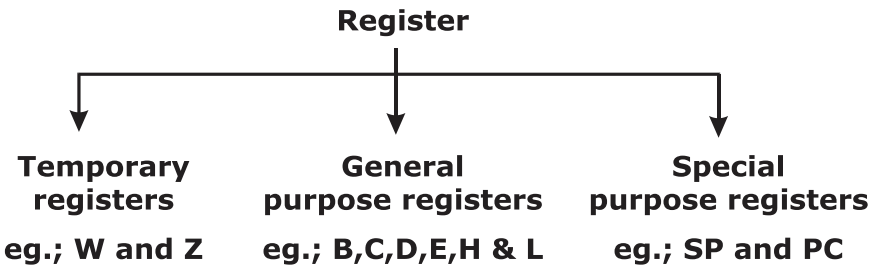
Sign Flag (S): Sign Flag is set if bit of the result is 1. Otherwise, it is reset.

Program counter (PC): It is used to store the l6 bit address of the next byte to be fetched from the memory or address of the next instruction to be executed.

Stack Pointer (SP): It is 16-bit register used as a memory pointer. It points to memory location in Read/Write memory which is called as stack.

REGISTER ARRAY

The register array can be categorized as:



8085 Signals:

Address lines: There are 16 address line AD_0 – AD_7 and A_8 ☐☐A_{15} to identify the memory locations.

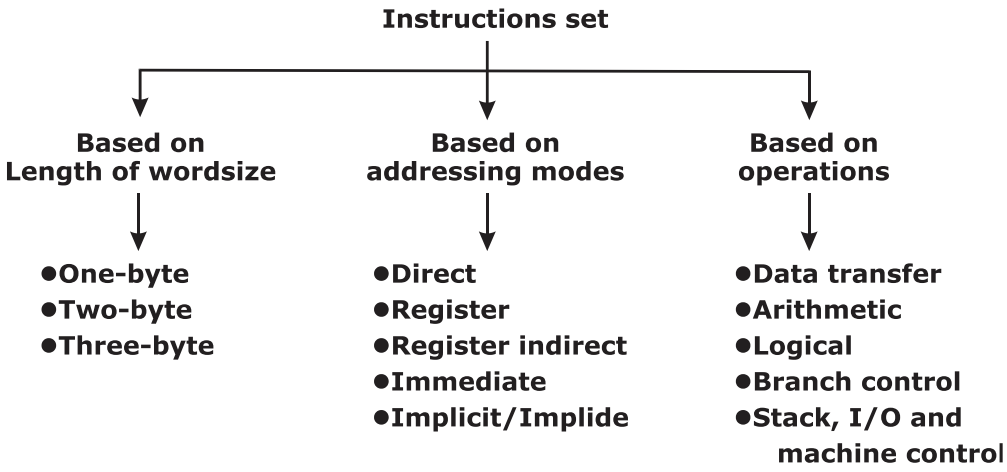
- In memory mapped input ; input Devices are treated as memory locations. You can connect max of 65536 devices in this technique.
- In input mapped input, input devices are identified by separate 8-bit address, same address can be used to identify input & output device.
- Max of 256 input & 256 output devices can be connected.

Programmable Interfacing Devices:

- 8185 → Programmable peripheral interface with 256 bytes RAM and 16-bits counter.
- 8255 → Programmable interface adaptor.
- 8253 → Programmable interval timer.
- 8251 → Programmable Communication Interfacing Device (USART).
- 8257 → Programmable DMA controller (4-channel)
- 8259 → Programmable Interrupt controller
- 8272 → Programmable Floppy Disk controller.
- CRT controller
- Key board and Display interfacing Device.

	CALL & RET	PUSH & POP
1.	When CALL executes, µp automatically stores 16 bits address of instruction next to CALL on the stack.	Programmer use PUSH to save the contents rp on stack.
2.	CALL executed, SP decremented by 2	PUSH executes "SP" decremented by "2"
3.	RET transfers contents of top 2 of SP to PC	Same here but to specific "rp".
4.	RET executes "SP" incremented by 2.	Same here

CLASSIFICATION OF INSTRUCTIONS SET OF 8085 MICROPROCESSOR



9.1. Symbols and Abbreviations used in Instruction Sets:

S.No.	Symbol/ Abbreviations	Meaning
1.	Address	16-bit address of the memory location
2.	Data	8-bit data
3.	Data 16	16-bit data
4.	R, R_1, R_2	One of the registers A, B, C, D, E, H and L
5.	A	Accumulator
6.	HL	Register pair HL
7.	BC	Register pair BC
8.	DE	Register pair DE
9.	PSW	Program Status Word

10.	M	Memory content/ locations whose address is in HL pair
11.	H	Appearing at the end of a group of digits specifies hexadecimal number
12.	R_p	One of the register pair. B represents BC pair; B is high order register and C is low order register
13.	R_H	The high order register of a register pair
14.	R_L	The low order register of a register pair
15.	PC	16-bit program counter, PCH is high order 8-bits and PCL is low order 8-bits of register PC
16.	CS	Carry Status
17.	[]	The contents of a register identified within the bracket
18.	[[]]	The contents of the memory location whose address is in the register pair identified within brackets
19.	^	AND operation
20.	v	OR operation
21.	$\forall$ or $\oplus$	Exclusive-OR operation
22.	$\leftarrow$	Move data in the direction of arrow
23.	$\Leftrightarrow$	Exchange contents
24.	A, B, C, D, E, H, L	8-bit register

Rotate Instruction:

RLC: Each bit shifted to adjacent left position. D_7 becomes D_0.

CY flag modified according to D_7.

RAL: Each bit shifted to adjacent left position. D_7 becomes CY and CY becomes D_0.

ROC: CY flag modified according D_0.

RAR: D_0 becomes CY and CY becomes D_7.

CALL and Return Instructions:

CALL – 18T states SRRWW

CC – Call on carry 9 – 18 states

CM – Call on minus 9-18

CNC – Call on no carry

CZ – Call on zero; CNZ call on non zero

CP – Call on +ve

CPE – Call on even parity

CPO – Call on odd parity

RET : 10T

RC :6/12 ‘t’ states

Jump Instruction:

JMP – 10T

JC – Jump on Carry 7/10T

States JNC – Jump on no carry

JZ – Jump on zero

JNZ – Jump on non zero

JP – Jump on positive

JM – Jump on Minus

JPE – Jump on even parity

JPO – Jump on odd parity.

- PCHL : Move HL to PC 6T
- PUSH: 12T ; POP : 10T
- SHLD: address : store HL directly to address 16T
- SPHL: Move HL to SP 6T
- STAX: R_p store A in memory 7T
- STC: Set carry 4T
- XCHG: exchange DE with HL “4T”

XTHL: Exchange stack with HL 16T

- For “AND” operation “AY” flag will be set and “CY” Reset
- For “CMP” if A < Reg/mem:

  $CY \rightarrow 1$ & $Z \rightarrow 0$ (Nothing but A – B)

  A > Reg/mem: $CY \rightarrow 0$ & $Z \rightarrow 0$

  A > Reg/mem: $Z \rightarrow 1$ & $Z \rightarrow 0$
- “DAD” Add HL + RP (10T) $\rightarrow$ fetching, busidle, busidle
- DCX, INX won’t effect any flags. (6T)
- DCR, INR effect all flags except carry flag. “CY” wont be modified
- “LHLD” load “HL” pair directly
- “RST” $\rightarrow$ 12T states
- SPHL, RZ, RNZ…, PUSH, PCHL, INX, DCX, CLL $\rightarrow$ fetching has 6T states
- PUSH – 12T; POP – 10T

Hardware Interrupts:

RST n	**Vectored address**
RST 4.5 (TRAP)	0024 H
RST5.5	002CH

RST 6.5	0034 H
RST 7.5	0036 H
INTR	Non-vectored

Apart from these hardware interrupts there are eight software interrupt present in 8085 microprocessor. All the software interrupts are vectored interrupt.

Software interrupts:

RST n	**Vectored address**
RST 0	0000H
RST 1	0008 H
RST 2	0010 H
RST 3	0018 H
RST 4	0020 H
RST 5	0028 H
RST 6	0030 H
RST 7	0038 H

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