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Rajasthan RVUNL

Electrical Engineering

Analog Electronics

100 Days Plan Formula Notes

ANALOG CIRCUITS (FORMULA NOTES/SHORT NOTES)

- Energy gap

$$\left.\begin{aligned} E_{G/Si} &= 1.21 - 3.6\times10^{-4}T \text{ ev} \\ E_{G/Gi} &= 0.785 - 2.23\times10^{-4}T \text{ ev} \end{aligned}\right\}$$

Energy gap depending on temperature

- $E_F = E_C - KT\ln\left(\frac{N_C}{N_D}\right) = E_V + KT\ln\left(\frac{N_V}{N_A}\right)$
- Number of electrons

$n = N_V e^{-(E_c - E_f)/RT}$ (KT in ev)

- Number of holes $p = N_V e^{-(E_f - E_v)/RT}$
- Mass action law $n_p = n_i^2 = N_C N_v\, e^{(EG/KT)}$
- Drift velocity $v_d = \mu E\left(\text{For si } v_d \le 10^7 \text{cm/sec}\right)$
- Hall voltage $v_H = \frac{BI}{w_e}$. Hall coefficient $R_H = \frac{1}{\rho}$.

ρ - charge density = qN_0 = ne…

- Conductivity, $\sigma = \rho\mu$; $\mu = \sigma R_H$.
- Maximum value of electric field @ junction $E_0 = \frac{q}{\epsilon_{si}} N_d \times n_{n0} = \frac{q}{\epsilon_{si}} N_A \times n_{p0}$.
- Charge storage @ junction

$Q_+ = -Q_- = qAx_{n0}N_D = qAx_{p0}N_A$

- Diffusion current densities, $J_p = -qD_p \frac{do}{dx}$ $J_n = -qD_n \frac{dn}{dx}$
- Drift current densities = $q(p\mu_p + n\mu_n)E$
- μ_p, μ_n decrease with increasing doping concentration.
- $\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{KT}{q} \approx 25 \text{ mv} @ 300K$
- Carrier concentration in N-type silicon $\mu_{n0} = N_D$; $p_{n0} = \frac{n_i^2}{N_D}$
- Carrier concentration in P-type silicon $p_{p0} = N_A$; $n_{p0} = \frac{n_i^2}{N_A}$
- Junction built in voltage $V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$
- Width of depletion region

$$W_{dep} = x_p + x_n = \sqrt{\frac{2\varepsilon_s}{N_A}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_R)} * \left(\frac{2\varepsilon ft}{q} = 12.93 \text{ m for si}\right)$$

- $\frac{x_n}{x_p} = \frac{N_A}{N_D}$
- Charge stored in depletion region

  $$q_J = \frac{aN_AN_D}{N_A+N_D} \times A \times W_{dep}$$

- Depletion capacitance,

  $$C_J = \frac{\varepsilon_s A}{W_{dep}}; \qquad C_{j0} = \frac{\varepsilon_s A}{W_{dep}/V_R} = 0$$

  $$C_j = \frac{C_{j0}}{\left(1+\frac{V_R}{V_0}\right)^m}$$

  $C_j = 2C_{j0}$ (for forward Bias)
- Forward current, $I = I_p + I_n$;

  $$I_p = Aqn_i^2 \frac{D_p}{L_pN_D}\left(e^{V/V_T}-1\right)$$

  $$I_n = Aqn_i^2 \frac{D_n}{L_nN_D}\left(e^{V/V_T}-1\right)$$

- Saturation current,

  $$I_s = Aqn_i^2\left(\frac{D_p}{L_pN_D}+\frac{D_n}{L_nN_D}\right)$$

- Minority carrier life time,

  $$\tau_p = \frac{L_p^2}{D_p}; \qquad \tau_n = \frac{L_n^2}{D_n}$$

- Minority carrier charge storage,

  $Q_p = \tau_p I_p, \qquad Q_n = \tau_p I_n$

  $Q = Q_p + Q_n = \tau_T I$, τ_T =Mean transist time
- Diffusion capacitance,

  $$C_d = \left(\frac{\tau_T}{hV_T}\right) I = \tau g \Rightarrow C_d \propto I.$$

  $\tau \rightarrow$ Carrier life time, g = Conductance = $\frac{I}{\eta V_T}$

- $I_{02} = 2^{(T_2-T_1)/10} I_{01}$
- Junction Barrier Voltage, $V_j = V_B = V_r$ (Open condition)
- $= V_r - V$ (Forward condition) $= V_r + V$ (Reverse condition)
- Probability of filled states above 'E'

  $$f(E) = \frac{1}{1+e^{(E-E_f)/KT}}$$

- Drift velocity of e^- $v_d \le 10^7$ cm/sec
- Poisson equation, $\frac{d^2V}{dx^2} = \frac{-\rho}{\epsilon} = \frac{-nq}{\epsilon} \Rightarrow \frac{dv}{dx} = E = \frac{-nqx}{\epsilon}$

Transistor:

- $I_E = I_{DE} + I_{nE}$
- $I_C = I_{CO} - \alpha I_E$ – Active region

  $I_C = -\alpha I_E + I_{CO}\left(1 - e^{V_C/V_T}\right)$

Common Emitter:

- $I_C = (1+\beta) I_{CO} + \beta I_B \quad \beta = \frac{\alpha}{1-\alpha}$
- $I_{CEO} = \frac{I_{Co}}{1-\alpha} \rightarrow$ Collector current when base open
- $I_{CEO} \rightarrow$ Collector current when $I_E = 0$, $I_{CBO} > I_{CO}$.
- $V_{BE,sat}$ or $V_{BC,sat}$ – 2.5 mV/°C;

  $V_{CE,sat} \rightarrow \frac{V_{BE,sat}}{10} = -0.25\ \text{mV/°C}$
- Large signal current gain, $\beta = \frac{I_C - I_{CBO}}{I_B + I_{CBO}}$
- DC current gain $\beta_{dc} = \frac{I_C}{I_B} = h_{FE}$
- $(\beta_{dc} = h_{FE}) \approx \beta$ when $I_B > I_{CBO}$
- Small signal current gain

  $\beta' = \left.\frac{\partial I_C}{\partial I_R}\right|_{V_{CE}} = h_{fe} = \frac{h_{FE}}{1 - (I_{CBO} + I_B)\frac{\partial h_{FE}}{\partial I_C}}$
- Over drive factor = $\frac{\beta_{active}}{\beta_{forced \rightarrow under\ saturation}}$

  $\because \quad I_{C,sat} = \beta_{forced} I_{B,sat}$

Conversion Formula:

$CC \leftrightarrow CE$

- $h_{ic} = h_{ie}$; $h_{rc} = 1$; $h_{fc} = -(1 + h_{fe})$; $h_{oc} = h_{oe}$

$CB \leftrightarrow CE$

- $h_{ib} = \frac{h_{ie}}{1+h_{fe}}; h_{ib} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}; h_{fb} = \frac{-h_{fe}}{1+h_{fe}}; h_{ob} = \frac{h_{oe}}{1+h_{fe}}$

Specifications of An Amplifier:

- $A_I = \frac{-h_f}{1+h_0Z_L}$ $Z_i = h_i + h_eA_IZ_L$ $A_{vs} = \frac{A_VZ_i}{Z_i+R_s} = \frac{A_IZ_L}{Z_i+R_S} = \frac{A_{I_s}Z_L}{R_S}$

  $A_V = \frac{A_IZ_L}{Z_i}$ $Y_0 = h_0 - \frac{h_fh_r}{h_i+R_s}$ $A_{Is} = \frac{A_VR_s}{Z_i+R_s} = \frac{A_{vs}R_s}{Z_L}$

Choice of Transistor Configuration:

- For intermediate stages CC can't be used as $A_V < 1$.
- CC can be used as output stage as it has low output impedance.
- CC/CB can be used as i/p stage because of i/p consideration.

Stability and Biasing:

Should be as min as possible

- For $S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BO},\beta}$ $S' = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\beta}$ $S'' = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{V_{BE},I_{CO}}$

  $\Delta I_C = S \times \Delta I_{CO} + S'\Delta V_{BE} + S''\Delta\beta$

- For fixed bias $S = \frac{1+\beta}{1-\beta\frac{dI_B}{dI_C}} = 1+\beta$

- Collector to Base bias

  $S = \frac{1+\beta}{1+\beta\frac{R_C}{R_C+R_B}}$ $0 < S < 1+\beta = \frac{1+\beta}{1+\beta\left(\frac{R_C+R_E}{R_C+R_E+R_B}\right)}$

- Self bias,

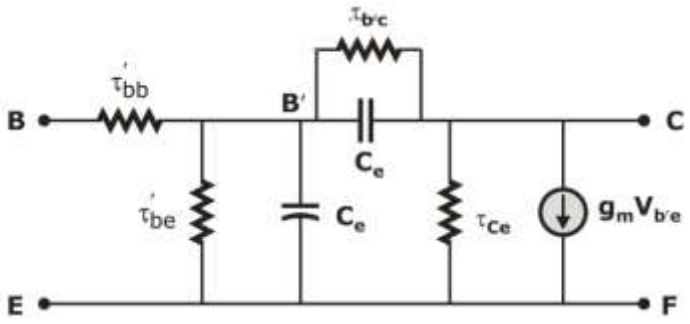
  $S = \frac{1+\beta}{1+\beta\frac{R_E}{R_E+R_{th}}} \approx 1+\frac{R_{th}}{R_e}$ $\beta R_E > 10R_2$

- $R_1 = \frac{V_{CC}R_{th}}{V_{th}}$; $R_2 = \frac{V_{CC}R_{th}}{V_{CC}-V_{th}}$

- For thermal stability

  $[V_{CC} - 2I_C(R_C + R_E)][0.07I_{CO} \times S] < \frac{1}{\theta}$; $V_{CE} < \frac{V_{CC}}{2}$

Hybrid – pi(π) – Model:

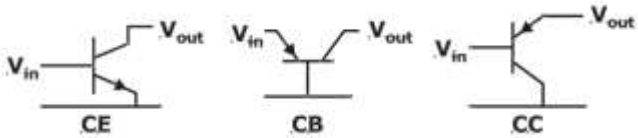


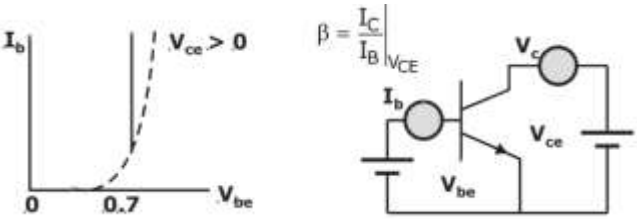
$$g_m = \frac{|I_C|}{V_T}$$

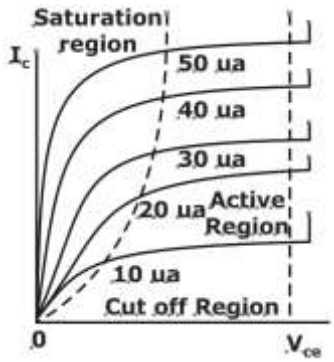
$$r_{b'e} = \frac{h_{fe}}{g_m}, \qquad r_{b'b} = h_{ie} - r_{b'e},\ r_{b'c} = \frac{r_{b'e}}{h_{re}}$$

$$g_{ce} = h_{oe} - (1 + h_{fe})\, g_{b'c}$$

- 3 Configurations are used on BJT, CE, CB and CC







COMPRESSION		
	BE	BC
SATURATION	f/b	f/b
ACTIVE	f/b	r/b
CUT OFF	r/b	r/b

AMPLIFIER COMPARISON			
	CB	CE	CF
R_i	LOW	MED	HIGH
A_I	A_I	β	β +1
A_V	High	High	<1
R_o	High	High	Low

For CE:

- $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} = \frac{g_m}{h_{fe} 2\pi(C_e + C_c)}$

- $f_T = h_{fe} f_\beta; \quad f_H = \frac{1}{2\pi r_{b'e} C} = \frac{g_{b'e}}{2\pi C},$

  $C = C_e + C_c(1 + g_m R_L)$

  f_T = SC current gain bandwidth product

  f_H = Upper cutoff frequency

For CC:

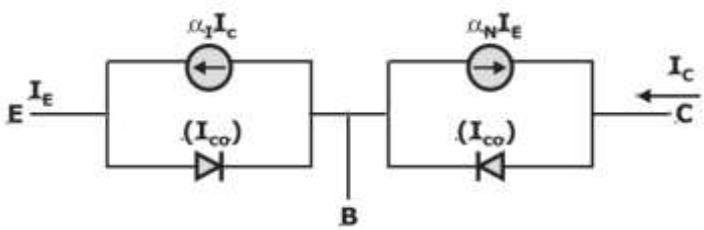
- $f_H = \frac{1 + g_m R_L}{2\pi C_L R_L} \approx \frac{g_m}{2\pi C_L} = \frac{f_T C_e}{C_L} = \frac{g_m + g_{b'e}}{2\pi(C_L + C_e)}$

For CC:

- $f_\alpha = \frac{1 + h_{fe}}{2\pi r_{b'e}(C_c + C_e)} = (1 + h_{fe}) f_\beta = (1 + \beta) f_\beta$

- $f_T = \frac{\beta}{1 + \beta} f_\alpha \qquad f_\alpha > f_T > f_\beta$

Ebress moll model:

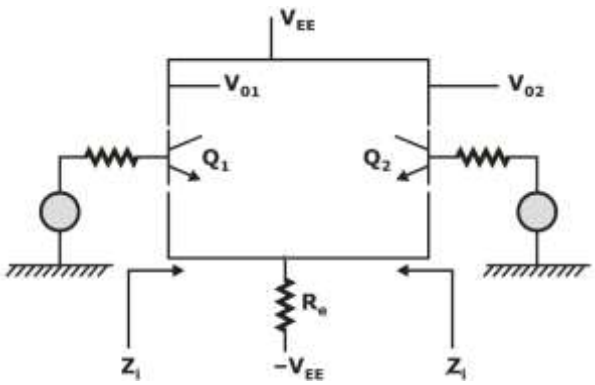


$I_C = -\alpha_N I_E + I_{CO}\left(1 - e^{V/V_T}\right)$

$I_E = -\alpha_I I_C + I_{EO}\left(1 - e^{V/V_T}\right)$

$\alpha_I I_{CO} = \alpha_N I_{EO}$

Multistage Amplifiers:



- $f_H^* = f_H\sqrt{2^{1/n}-1}$; $\quad f_H^* = \dfrac{f_L}{\sqrt{2^{1/n}-1}}$
- Rise time $r_r = \dfrac{0.35}{f_H} = \dfrac{0.35}{BW}$
- $r_r^* = 1.1\sqrt{t_{r1}^2 + t_{r2}^2 + \ldots}$
- $r_L^* = 1.1\sqrt{t_{L1}^2 + t_{L2}^2 + \ldots}$
- $\dfrac{1}{f_H^*} = 1.1\sqrt{f_{H1}^2 + f_{H2}^2 + \ldots}$

Differential Amplifier:

- $Z_i = h_{ie} + (1 + h_{fe})2R_e = 2h_{fe}R_e \approx 2\beta R_e$
- $g_m = \dfrac{\alpha_o |I_{EE}|}{4V_T} = \dfrac{I_C}{4V_T} = g_m \text{of} \dfrac{BJT}{4}$ $(\alpha_o \rightarrow$ DC value of $\alpha)$
- CMRR$= \dfrac{h_{fe}R_e}{R_s + h_{ie}}$; $R_e \uparrow, \rightarrow Z_i \uparrow, A_d \uparrow$ & CMRR $\uparrow$

Darlington Pair:

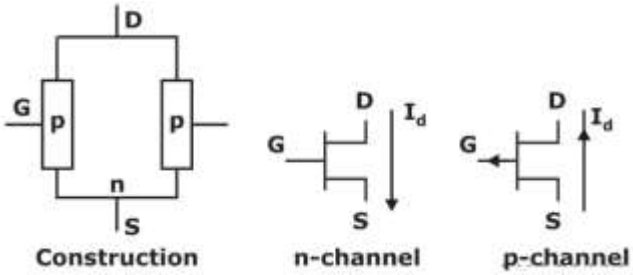
- $A_I = (1 + \beta_1)(1 + \beta_2)$; $A_V \approx 1(<1)$
- $Z_i = \dfrac{(1+h_{fe})^2 R_{ez}}{1 + h_{fe}h_{oc}R_{e2}}\Omega$

  [If Q_1 and Q_2 have same type] $= A_I R_{e2}$
- $R_o = \dfrac{R_s}{(1+h_{fe})} + \dfrac{2h_{ie}}{(1+h_{fe})}$
- $g_m = (1 + \beta_2)g_{m1}$

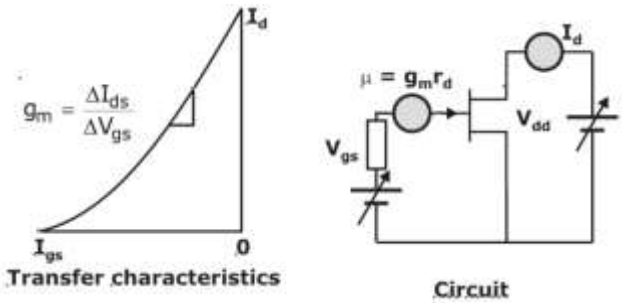
Tuned Amplifiers: (Parallel Resonant ckts used):

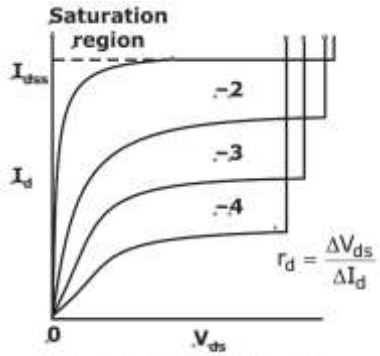
- $f_0 = \frac{1}{2\pi\sqrt{LC}}$ $\quad Q \rightarrow$ 'Q' factor of resonant ckt which is very high
- $BW = \frac{f_0}{Q}$
- $f_L = f_0 - \frac{\Delta BW}{2}$
- $f_H = f_0 - \frac{\Delta BW}{2}$
- For double tuned amplifier 2 tank circuits with same f_0 used. $f_0 = \sqrt{f_L f_H}$.

FIELD EFFECT TRANSISTOR, FET IS UNIPOLAR DEVICE



- S = Source, G = Gate, D = Drain
- GS Junction in Reverse Bias Always
- V_{gs} Controls Gate Width
- VI Characteristics

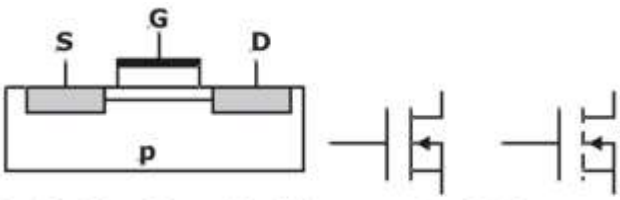




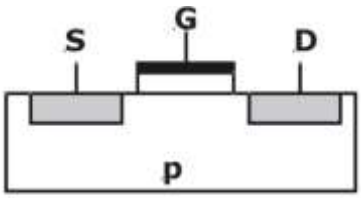
Forward Characteristics

- Shockley equation
- $I_d = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2, \quad g_m = g_{m0}\left(1 - \frac{V_{gs}}{V_p}\right)$

MOSFET (Metal Oxide Semiconductor FET, IGFET)



Deplection Type Mosfet Symbols



Enhancement Mosfet

- Depletion Type MOSFET can work width $V_{gs} > 0$ and $V_{gs} < 0$
- Enhancement MOSFET operates with $V_{gs} > V_t$, V_t = Threshold Voltage
- NMOSFET formed in p-substrate
- If $V_{GS} \geq V_t$ channel will be induced and i_D (Drain $\rightarrow$ Source)
- $V_t \rightarrow +$ve NMOS
- $i_D \propto (V_{GS} - V_t)$ for small V_{DS}
- $V_{DS} \uparrow \rightarrow$ channel width @ drain reduces.
- $V_{DS} = V_{GS} - V_t$ channel width $\approx 0 \rightarrow$ pinch off further increase no effect.

- For every $V_{GS} > V_t$ there will be $V_{DS,sat}$
- $i_D = K_n'\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2\right]\left(\frac{W}{L}\right) \rightarrow$

  triode region ($V_{DS} < V_{GS} - V_t$)

  $K_n' = \mu_n C_{ox}$
- $i_D = \frac{1}{2}K_n'\left(\frac{W}{L}\right)\left[V_{DS}^2\right] \rightarrow$ saturation
- $r_{DS} = \dfrac{1}{K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)} \rightarrow$ Drain to source resistance in triode region

PMOS:

- Device operates in similar manner except V_{GS}, V_{DS}, V_t are -Ve
- i_D enters @ source terminal & leaves through Drain.

  $V_{GS} \le V_t \rightarrow$ induced channel, $V_{DS} \ge V_{GS} - V_t \rightarrow$ Continuous channel

  $i_D = K_p'\left(\frac{W}{L}\right)\left[(V_{GS} - V_t)^2 - \frac{1}{2}V_{DS}^2\right]$ $K_p' = \mu_p C_{ox}$

  $V_{DS} \le V_{GS} - V_t \rightarrow$ Pinched off channel.
- NMOS devices can be made smaller and thus operates faster. Required low power supply.
- Saturation region $\rightarrow$ amplifier.
- For switching operation Cutoff and triode region are used.

NMOS	PMOS	
$V_{GS} \ge V_t$	$V_{GS} \le V_t$	$\rightarrow$ Induced channel
$V_{GS} - V_{DS} > V_t$	$V_{GS} - V_{DS} < V_t$	$\rightarrow$ Continuous channel (Triode region)
$V_{DS} \ge V_{GS} - V_t$	$V_{DS} \le V_{GS} - V_t$	$\rightarrow$ Pinchoff (Saturation)

Depletion Type MOSFET:

[Channel is physically implanted. i_0 flows with $V_{GS} = 0$]

- For n-channel

  $V_{GS} \rightarrow +$ve $\rightarrow$ enhances channel
  $\rightarrow -$ve $\rightarrow$ depletes channel
- $i_D - V_{DS}$ characteristics are same except that V_t is –ve for n-channel.

- Value of Drain current obtained in saturation when $V_{GS} = 0 \Rightarrow I_{DSS}$.

$$\because\ I_{DSS} = \frac{1}{2}K_n' \left(\frac{W}{L}\right)V_t^2.$$

MOSFET as Amplifier:

- For saturation $V_D > V_{GS} - V_t$
- To reduce non linear distortion $v_{gs} \ll 2(V_{GS} - V_t)$
- $i_D = K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)v_{gs} \Rightarrow g_m = K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)$
- $\frac{v_d}{v_{gs}} = -g_m R_D$
- Unity gain frequency, $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$

JEET:

- $V_{GS} \le V_p \Rightarrow i_D = 0 \rightarrow$ Cut off
- $V_p \le V_{GS} \le 0,\ V_{DS} \le V_{GS} - V_p$
- $i_D = I_{DSS}\left[2\left(1 - \frac{V_{GS}}{V_p}\right)\left(\frac{V_{DS}}{-V_p}\right) - \left(\frac{V_{DS}}{V_p}\right)^2\right] \rightarrow$ Triode
- $V_p \le V_{GS} \le 0,\ V_{DS} \ge V_{GS} - V_p$

$$\left.\begin{aligned} i_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \Rightarrow V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \\ g_m &= \frac{2I_{DSS}}{|V_p|}\left(1 - \frac{V_{GS}}{V_p}\right) = \frac{2I_{DSS}}{|V_p|}\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \end{aligned}\right\} \rightarrow \text{Saturation}$$

Operational Amplifier: (VCVS)

- Fabricated with VLSI by using epitaxial method.
- High input impedance, Low output impedance, High gain, Bandwidth, slew rate.
- FET is having high input impedance compared to op-amp.
- Gain Bandwidth product is constant.
- Closed loop voltage gain

$$A_{CL} = \frac{A_{OL}}{1 \pm \beta A_{OL}} \quad \beta \rightarrow \text{Feed back factor}$$

- $\Rightarrow V_0 = \frac{-1}{RC}\int V_i dt \rightarrow$ LPF acts a integrator:
- $\Rightarrow V_0 = \frac{-R}{L}\int V_i dt; \qquad V_0 = \frac{-L}{R}\frac{dv_i}{dt}$ (HPF)
- For OP-amp integrator, $V_0 = \frac{-R}{L}\int V_i dt;$

  Differentiator, $V_0 = -\tau\frac{dv_i}{dt}$
- Slew rate SR = $\frac{\Delta v_0}{\Delta t} = \frac{\Delta v_0}{\Delta t} \times \frac{\Delta v_i}{\Delta t} - A \times \frac{dv_i}{\Delta t}$
- Maximum operating frequency

  $$f_{max} = \frac{\text{Slew rate}}{2\pi\Delta V_0} = \frac{\text{Slew rate}}{2\pi \times \Delta V_i \times A}$$
- In voltage follower voltage series feedback.
- In non inverting mode voltage series feedback.
- In inverting mode voltage shunt feed back.
- $V_0 = -\eta V_T \ln\left(\frac{V_i}{RI_0}\right)$
- $V_0 = -V_{BE} = -\eta V_T \ln\left(\frac{V_s}{RI_{CO}}\right)$
- Error in differential %error = $\frac{1}{CMRR}\left(\frac{V_c}{V_d}\right) \times 100\%$

Power Amplifier:

- Fundamental power delivered to load

  $$P_1 = \left(\frac{B_2}{\sqrt{2}}\right)^2 R_L = \frac{B_1^2}{2} R_L$$
- Total Harmonic power delivered to load,

  $$P_T = \left[\frac{B_1^2}{2} + \frac{B_2^2}{2} + \ldots\right] R_L = P_1\left[1 + \left(\frac{B_2}{B_1}\right)^2 + \left(\frac{B_3}{B_1}\right)^2 + \ldots\right] \quad P_T = [1 + D^2]\, P_1$$

Where, $D = \sqrt{+D_2^2 + \ldots + D_n^2}$, $D_n = \frac{B_n}{B_1}$

D = Total harmonic distortion.

Class A operation:

- Output I_C flows for entire 360.°
- 'Q' point located @ centre of DC load line i.e., $V_{ce} = \frac{V_{cc}}{2}$; $\eta = 25\%$
- Min Distortion, min noise interference, eliminates thermal run way.
- Lowest power conversion efficiency and introduce power drain.
- $P_T = I_C V_{CE} - I_C V_{ce}$ if $i_C = 0$, it will consume more power.
- P_T is dissipation in single transistors only (single ended).

Class B:

- I_C flows for 180°, 'Q' located @ cutoff; η = 78.5%; eliminates power drain.
- Higher Distortion, more noise interference, introduce cross over distortion.
- Double ended. i.e., 2 transistors. $I_C = 0$ [transistors are connected in that way]

  $P_T = i_C V_{ce}$
- $P_T = i_C V_{ce} = 0.4P_0$, $P_T \rightarrow$ power dissipated by 2 transistors.

Class AB operation:

- I_C flows for more than 180° and less than 360°.
- 'Q' located in active region but near to cutoff; η = 60%.
- Distortion and Noise interference less compared to class 'B' but more in compared to class 'A'.
- Eliminates cross over Distortion.

Class 'C' Operation:

- I_C flows for < 180°; 'Q' located just below cutoff; η = 87.5%.
- Very rich in Distortion; noise interference in high.

Oscillators:

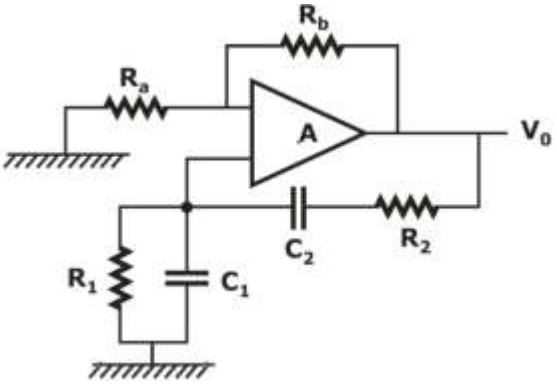
- For RC phase shift oscillator, $f = \frac{1}{2\pi RC\sqrt{6 + 4K}}$

  $h_{fe} \geq 4k + 23\frac{29}{k}$, where $k = \frac{R_C}{R}$

$$f = \frac{1}{2\pi RC\sqrt{6}}, \quad \mu > 29$$

- For op-amp RC oscillator, $f = \frac{1}{2\pi RC\sqrt{6}} |A_f| 29 \Rightarrow R_f \geq 29R_1$

Wein Bridge Oscillator:

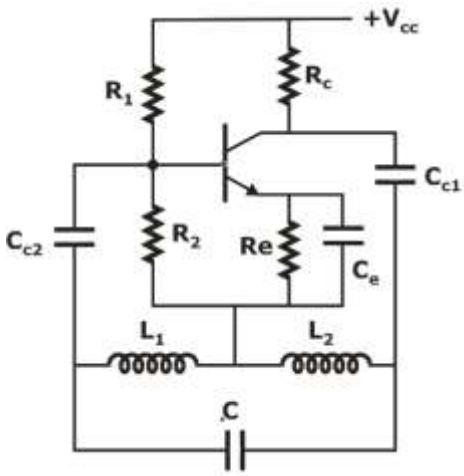


$$f = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}},$$

If $R_1 = R_2 = R$, $C_1 = C_2 = C$,

$$f = \frac{1}{2\pi Rc}, A = \frac{1}{\beta} = 3$$

Hartley Oscillator:



$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}} \qquad |h_{fe}| \geq \frac{L_2}{L_1}$$

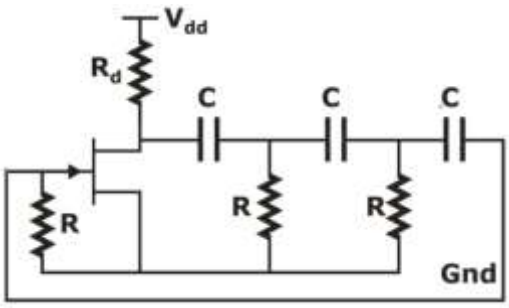
$$|\mu| \geq \frac{L_2}{L_1}, \qquad |A| \geq \frac{L_2}{L_1} \rightarrow \frac{R_f}{R_1}$$

Colpits Oscillator:

$$f = \frac{1}{2\pi\sqrt{L\left(\frac{C_1C_2}{C_1 + C_2}\right)}} \qquad |h_{fe}| \geq \frac{C_1}{C_2}$$

$$|\mu| \geq \frac{C_1}{C_2}, \qquad |A| \geq \frac{C_1}{C_2}$$

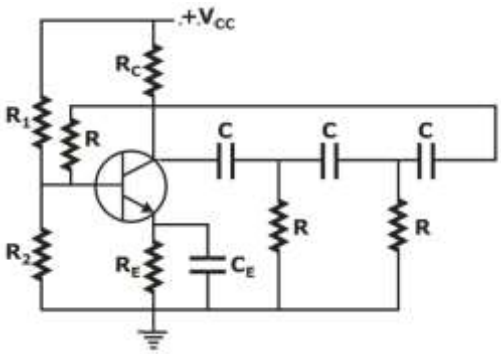
Phase Shift Oscillator:



FET MODEL

$$f = \frac{1}{2\pi\sqrt{6RC}}, \quad A = 29,$$

Minimum RC sections 3



BJT MODEL

$$f = \frac{1}{2\pi RC\sqrt{6 + \left(\frac{4R_C}{R}\right)}}, \quad A = 29,$$

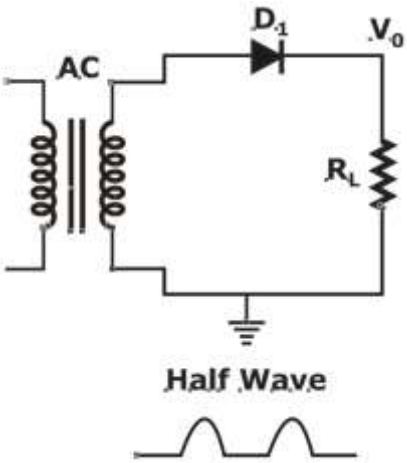
Minimum RC sections 3.

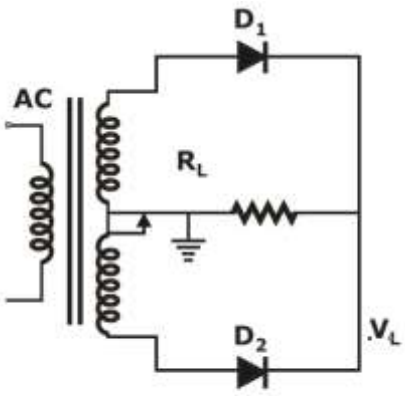
Comparisons	
BJT	**FET**
Current controlled	Voltage controlled
High gain	Med gain

Bipolar	Unipolar
Temp sensitive	Little effect of T
High GBWP	Low GBWP

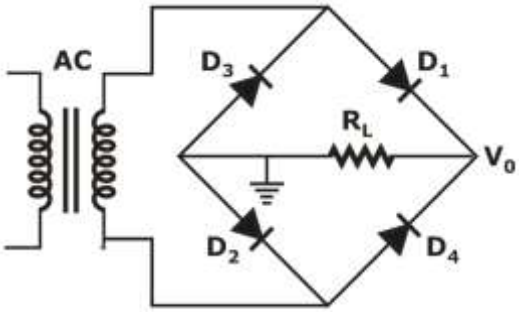
MOSFET	JPET
High, $R_i = 10^{10}$	-10^8
$R_0 = 50\ k\Omega$	$\geq 1\ m\Omega$
Depletion enhancement mode	Depletion mode
Delicate	Rugged

Rectifiers:





Full Wave



Bridge

Comparisons:

	HW	FE CT	FW BR
V_{DC}	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
V_{rms}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
γ (Ripple factor)	1.21	0.482	0.482
η (Ripple factor)	40.6%	81%	81%
PIV Peak Inverse Voltage	V_m	$2V_m$	V_m

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