

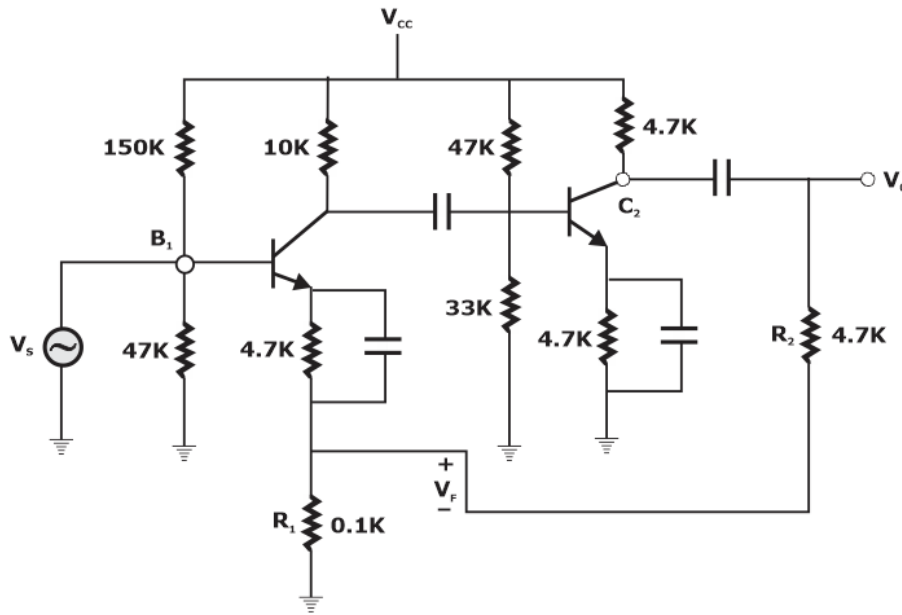
# ESE Mains Achiever's Study Plan

Electronics & Communication Engineering

Analog Circuits Part-2



1. A two stage Feedback amplifier is shown below. Transistor parameters are  $h_{fe} = 50$ ,  $h_{ie} = 1.1k\Omega$ ,  $h_{re} = h_{oe} = 0$ . Calculate  $A_{Vf}$ ,  $R_{Of}$ ,  $R_{if}$ .



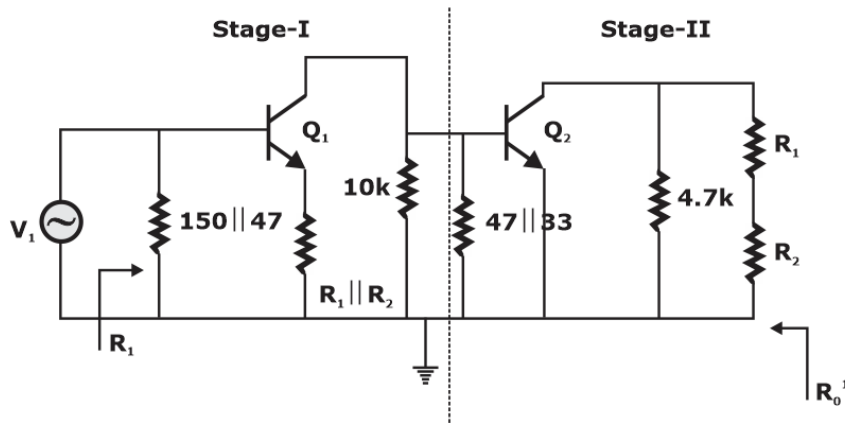
**Sol. Step 1:**  $R_1$  &  $R_2$  form voltage divider & they constitute Feedback network. This network creates voltages-series Feedback.

$$A = A_v = \frac{V_o}{V_s}$$

**Step 2:**

If output node G is grounded, then  $R_1$  &  $R_2$  appear in parallel in the input circuit.

If input loop is broken, then  $R_1$  &  $R_2$  appear in series in the output circuit.



**Step 3:**  $\beta = ?$

$V_o$  gets divides between  $R_1$  &  $R_2$ .

$$\text{Hence, } V_f = \frac{V_o R_1}{R_1 + R_2}$$

$$\frac{V_f}{V_o} = \beta = \frac{R_1}{R_1 + R_2} = \frac{0.1}{0.1 + 4.7} = \frac{1}{48}$$

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**Step 4:** If required then replace Transistor with appropriate small signal model.

**Step 5:** Calculate gain without Feedback, input & output impedences without feedback.

Q<sub>2</sub> CE amplifier with Bypass C

$$A_{V_2} = \frac{-h_{fe} R_L^1}{h_{ie}}$$

$$R_L^1 = 4.7 \parallel 4.7 = 2.37K$$

$$= \frac{-50 \times 2.37}{1.1}$$

$$= -107.7$$

$$R_{i_2}^1 = 47 \parallel 33 \parallel h_{ie} = 47 \parallel 33 \parallel 1.1$$

$$= 1.05 K \Omega$$

$$R_{L1}^1 = 10 \parallel R_{i_2}^1 = 10 \parallel 1.05$$

$$= 0.95 K \Omega$$

Q<sub>1</sub>: CE amplifier with un-bypassed resistance

$$(R_1 \parallel R_2) = R_E = 0.098K \Omega$$

$$A_{V_1} = \frac{-h_{fe} / R_L^1}{h_{ie} + (1 + h_{fe}) R_E}$$

$$= \frac{-50 \times 0.95}{1.1 + 51 \times 0.098}$$

$$= -7.78$$

$$\frac{V_o}{V_s} = A_V = A_{V_1} \times A_{V_2} = -7.78 \times (-107.7) = 838$$

$$R_i = 150 \parallel 47 \parallel [h_{ie} + (1 + h_{fe}) R_E]$$

$$= 150 \parallel 47 \parallel 6.09$$

$$= 5.21 K \Omega$$

$$R_{O1} = 4.7 \parallel 4.8$$

$$= 2.37 K \Omega$$

**Step 6:**  $D = 1 + \beta A = ?$

$$D = 1 + \beta A_V = 1 + \frac{1}{48} \times 838 = 18.46$$

**Step 7:**

$$D = 1 + \beta A_V = 1 + \frac{1}{48} \times 838 = 18.46$$

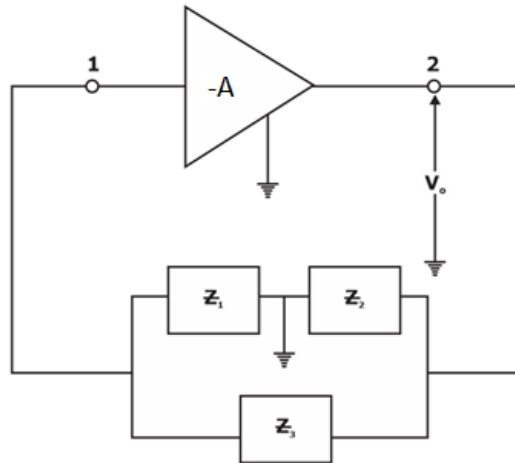
$$A_{VF} = \frac{A_V}{1 + \beta A_V} = \frac{838}{18.46} = 45.4$$

$$R_{iF} = R_i \times D = 5.21 \times 18.46 = 96.17 k \Omega$$

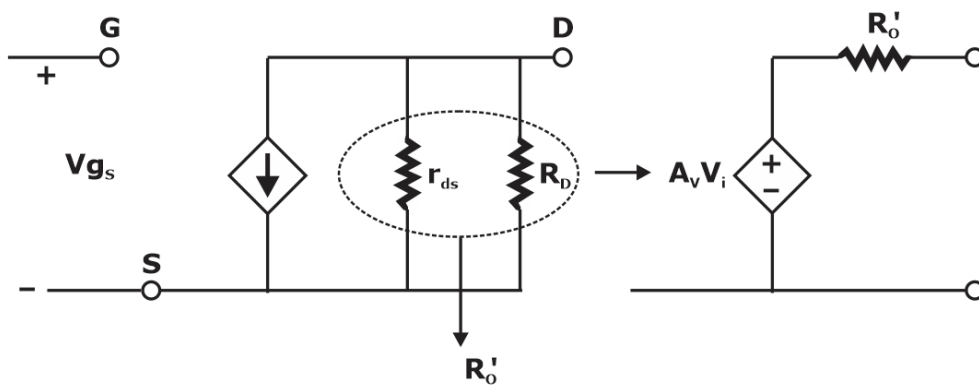
$$R_{O1F} = \frac{R_{O1}}{D} = \frac{2.37}{18.46} = 0.128 K \Omega$$

2. Derive the condition for LC oscillations in basic feedback amplifier.

Sol. Consider the basic amplifier having gain A and with the feedback network as shown below:

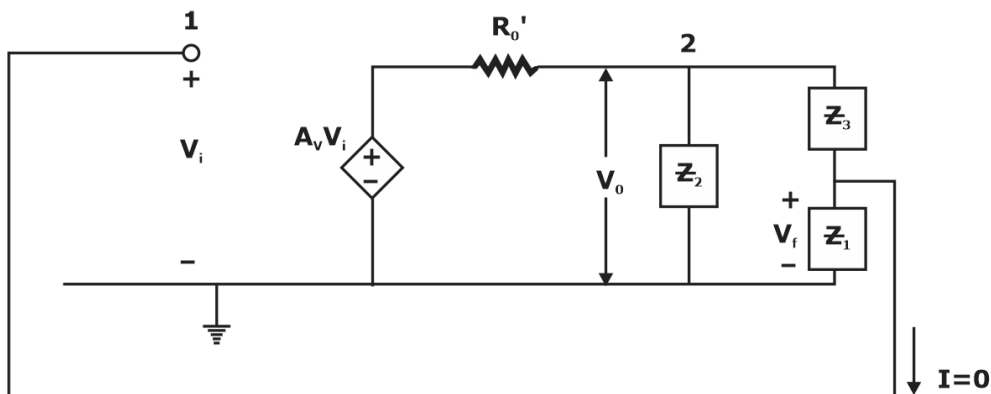


Consider it to be FET amplifier and has a small signal model as shown:



# Analysis:-

LC oscillator can be redrawn by replacing the amp block with it's equivalent circuit.



If the effect of feedback network is considered, then net load for amplifier will be  $Z_L \Rightarrow$

$$Z_L = Z_2 \parallel (Z_1 + Z_3)$$

$$Z_L = \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$$

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$A_v V_i$  gets divided into  $R_o^1$  &  $Z_L$

$$V_o = \frac{A_v \cdot V_i \cdot Z_L}{R_o^1 + Z_L}$$

$$\frac{V_o}{V_i} = A = \frac{A_v \cdot Z_L}{R_o^1 + Z_L}$$

$$A = A_v \cdot \frac{\frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}}{R_o^1 + \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}}$$

$$A = \frac{A_v \cdot Z_2 (Z_1 + Z_3)}{Z_2 (Z_1 + Z_3) + R_o^1 (Z_1 + Z_2 + Z_3)}$$

$V_o$  gets divided between  $Z_3$  &  $Z_1$

$$V_f = \frac{V_o \cdot Z_1}{Z_1 + Z_3}$$

$$\frac{V_f}{V_o} = \beta = \frac{Z_1}{Z_1 + Z_3} \dots\dots(2)$$

Loop gain =  $A \times \beta$

$$= \frac{A_v \cdot Z_1 \cdot Z_2}{R_o^1 (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)}$$

Put  $Z_1 = jX_1, Z_2 = jX_2, Z_3 = jX_3$

Consider only purely reactive components

$$\text{Loop gain} = \frac{-A_v X_1 X_2}{jR_o^1 (X_1 + X_2 + X_3) - X_2 (X_1 + X_3)} \dots\dots(3)$$

At  $\omega_o$ , phase of loop gain should be  $360^\circ$

$$\text{Hence, } R_o^1 (X_1 + X_2 + X_3) = 0$$

$$X_1 + X_2 + X_3 = 0 \text{ at } \omega = \omega_o$$

Condition for oscillation to occur

At  $\omega = \omega_o$ ,

$$\text{Loop gain} = \frac{-A_v X_1 X_2}{j0 - X_2 (X_1 + X_3)} = \frac{A_v X_1}{X_2}$$

For sustained oscillation;  $|\text{loop gain}| \geq 1$

$$|A_v| \frac{X_1}{X_2} \geq 1$$

$$|A_v| \geq \frac{X_2}{X_1}$$

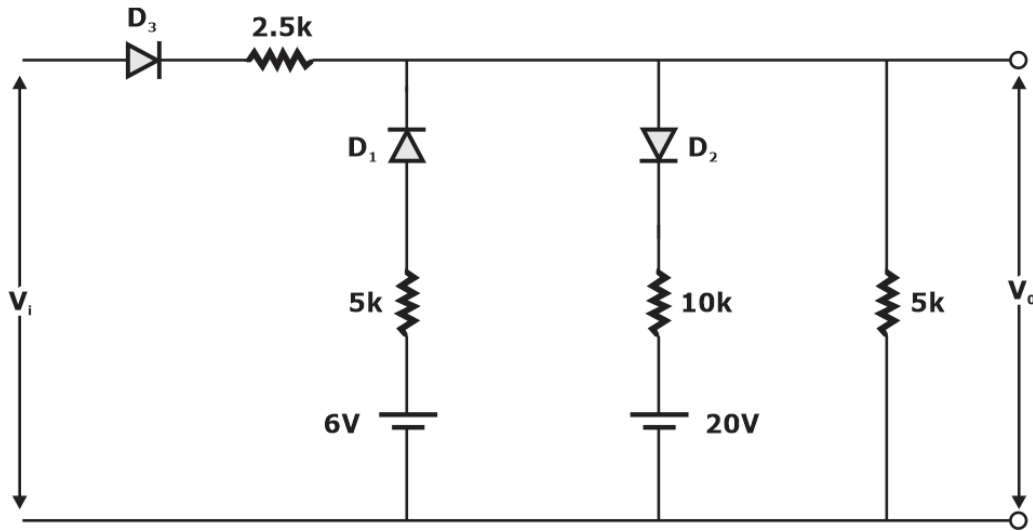
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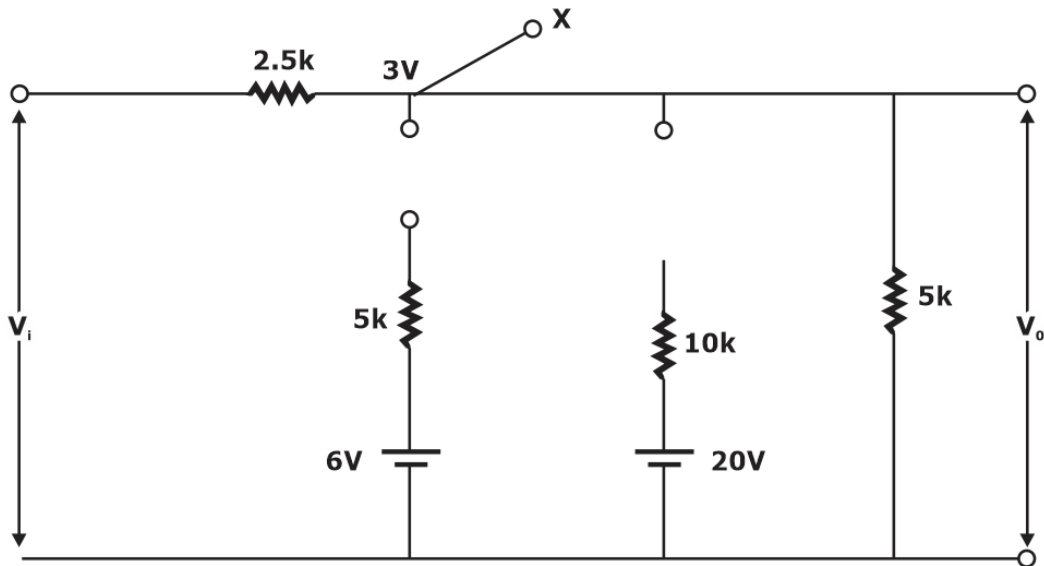
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3. In the circuit shown below diodes are ideal, input is varied from 0 to 50V. Plot transfer characteristics.



Sol.



Let  $D_1, D_2$  &  $D_3$  be off

→  $V_x = 0$  initially but as  $D_1$  is ON

$$\text{Then } V_x = \frac{5}{5+5} \times 6 = 3V$$

**(a)**  $V_i < 3V$ :  $D_3 \rightarrow$  OFF,  $D_2 \rightarrow$  OFF

&  $D_1 \rightarrow$  ON

$$V_o = V_x = 3V$$

**(b)** If  $V_i > 3V$ :  $D_3 \rightarrow$  ON

KCL at X:

$$\frac{V_i - V_x}{2.5} + \frac{6 - V_x}{5} = \frac{V_x - 0}{5}$$

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$$2V_i - 2V_x + 6 - V_x = V_x$$

$$V_x = \frac{2V_i + 6}{4} = \frac{V_i + 3}{2}$$

D<sub>1</sub> remains On, if

$$V_x < 6$$

$$\frac{V_i + 3}{2} < 6$$

$$V_i < 9V$$

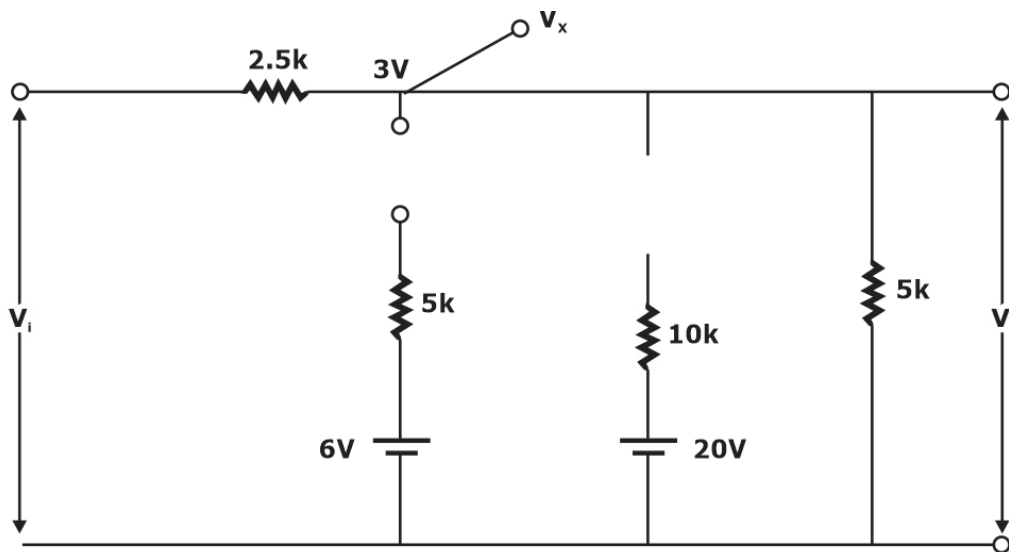
**(c)**  $3 < V_i < 9$ : D<sub>1</sub> & D<sub>3</sub> are ON

D<sub>2</sub> = OFF

$$V_o = V_x = \frac{V_i + 3}{2}$$

**(d)**  $V_i > 9$ : D<sub>1</sub> → OFF

Let D<sub>2</sub> be OFF



$$V_x = \frac{5}{2.5 + 5} \times V_i$$

$$V_x = \frac{2}{3} V_i$$

D<sub>2</sub> remains off  $V_x < 20$

$$\frac{2V_i}{3} < 20$$

$$V_i = 30V$$

(i) If  $9 < V_i < 30$  : - D<sub>1</sub> & D<sub>2</sub> → OFF

$$D_3 \text{ is ON \& } V_o = V_x = \frac{2}{3} V_i$$

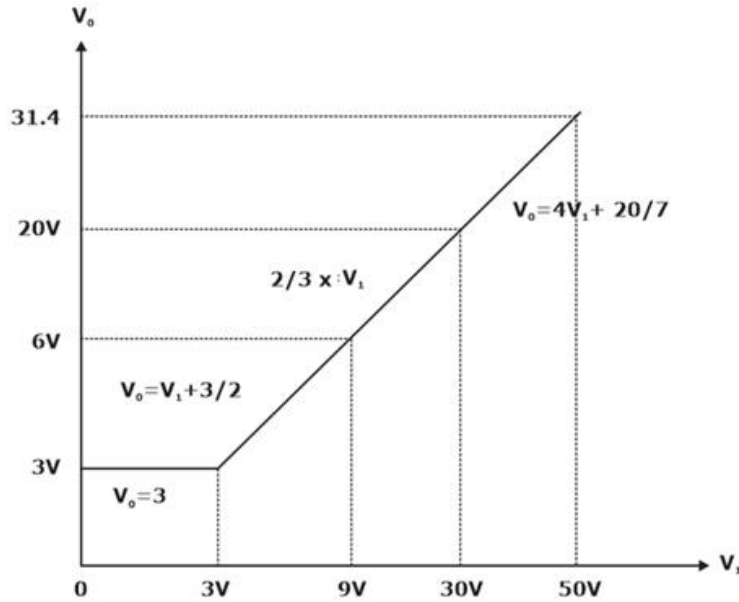
(ii) If  $V_i > 30$ :  $D_2$  becomes ON

$D_3$  is ON

$D_1$  is OFF

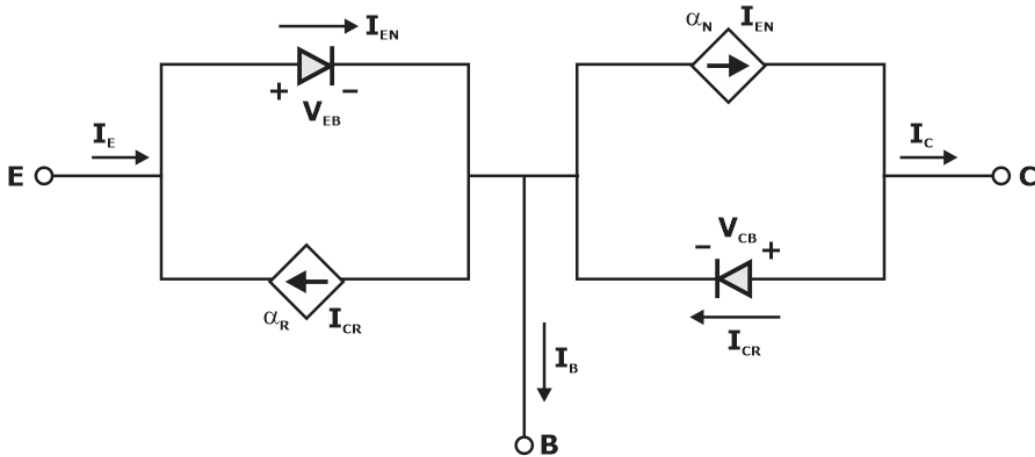
$$\text{KCL at X: } \frac{V_i - V_x}{2.5} = \frac{V_x - 20}{10} + \frac{V_x}{5}$$

$$V_x = \frac{4V_i + 20}{7}$$



4. Explain the BJT model using Eber-molls model.

Sol. Ebers- moll model of BJT: consider Coupled diode model for PNP transistor



→ The two diodes represent  $J_E$  &  $J_C$ .

→  $I_{EN}$  is the current through emitter  $J_E$  in normal active mode.

$$I_{EN} = I_{ES} (e^{V_{EB}/VT} - 1)$$

→  $I_{CR}$  → current through collector  $J_C$  in reverse active mode.

$$I_{CR} = I_{CS} (e^{V_{CB}/VT} - 1)$$

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→ Dependent source  $\alpha_N I_{EN}$  represents current through collector Junction in normal active mode.

→ Dependent source  $\alpha_R I_{CR}$  represents current through  $J_E$  in reverse active mode.

$\alpha_N$  = large signal current gain of normal active mode

$\alpha_R$  = large signal current gain of Reverse Active mode.

→  $\alpha_N \gg \alpha_R$  ( $\alpha_N \cong 1$  &  $\alpha_R$  signally greater than zero (Because BJT is unsymmetrical  $N_E \neq N_C$ ))

KCL at Emitter:

$$I_E + \alpha_R I_{CR} = I_{EN}$$

$$I_E = I_{EN} - \alpha_R I_{CR} \dots \dots \dots (1)$$

$$I_E = I_{ES} (e^{V_{EB}/V_T} - 1) - \alpha_R I_{CS} (e^{V_{CB}/V_T} - 1) \dots \dots \dots (2)$$

KCL at collector:-

$$I_C + I_{CR} = \alpha_N I_{EN}$$

$$I_C = \alpha_N I_{EN} - I_{CR} \dots \dots \dots (3)$$

$$I_C = \alpha_N I_{ES} (e^{V_{EB}/V_T} - 1) - I_{CS} (e^{V_{CB}/V_T} - 1) \dots \dots \dots (4)$$

$$I_B = I_E - I_C \text{ by equation (2)-(4)}$$

$$I_B = (1 - \alpha_N) I_{ES} (e^{V_{EB}/V_T} - 1) + (1 - \alpha_R) I_{CS} (e^{V_{CB}/V_T} - 1) \dots \dots \dots (5)$$

Eqn. (2), (4) & (5) are known as equation they can be used to calculate  $I_E$ ,  $I_C$  &  $I_B$  for all modes of operation.

Combine eqn. (1) & (3) →

$$I_E = I_{EN} - \alpha_R (\alpha_N I_{EN} - I_{CR})$$

$$I_E = (1 - \alpha_R \cdot \alpha_N) I_{EN} + \alpha_R I_{CR}$$

$$I_E = (1 - \alpha_R \cdot \alpha_N) I_{ES} [e^{V_{EB}/V_T} - 1] + \alpha_R I_{CR}$$

$$I_E = I_{EO} [e^{V_{EB}/V_T} - 1] + \alpha_R I_{CR} \dots \dots \dots (6)$$

When  $I_{EO} = (1 - \alpha_R \alpha_N) I_{ES}$ .

$I_{EO}$  - called Reverse saturation current of emitter Junction. When collector terminal is open circuited.

Form eqn. (3):

$$I_C = \alpha_N I_{EN} - I_{CR}$$

$$I_C = \alpha_N [I_E + \alpha_R I_{CR}] - I_{CR} \dots \dots \dots (\text{from (1)})$$

$$I_C = \alpha_N I_E - (1 - \alpha_N \alpha_R) I_{CR}$$

$$I_C = \alpha_N I_E - (1 - \alpha_N \alpha_R) I_{CS} (e^{V_{CB}/V_T} - 1)$$

$$I_C = \alpha_N I_E - I_{CO} (e^{V_{CB}/V_T} - 1) \dots \dots \dots (7)$$

$I_{CO}$  → Reverse saturation current of [where  $I_{CO} = (1 - \alpha_N \alpha_R) I_{CS}$ ]

Collection Junction when emitter is open Circuit.

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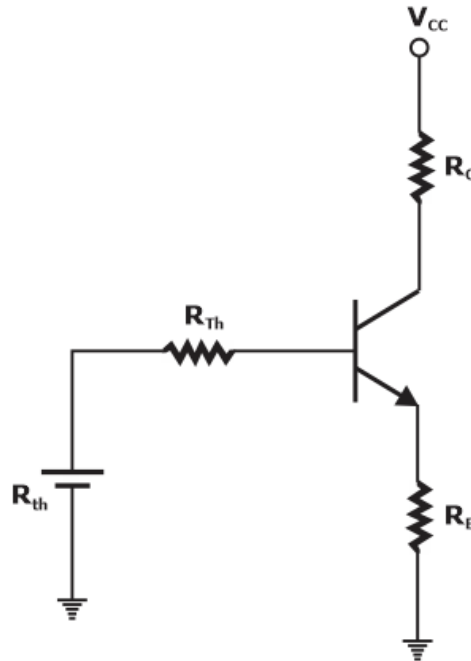
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5. BJT has  $\beta = 100$  &  $V_{BE} = 0.7$  Volt, Design self-bias circuit to operate BJT at  $V_{CE} = 6V$ ,  $I_C = 1.5$  mA. Assume stability factor  $S = 8$

Sol. **Step 1:** Draw simplified self-bias circuit



$$V_{Th} = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

Where  $V_{CC}$  is the voltage supply of the self bias circuit and  $R_1$  and  $R_2$  form self bias resistors.

**Step 2:** Calculate  $R_C$  &  $R_E$  by using KVL in collector loop

$$+V_{CC} - R_C I_C - V_{CE} - R_E I_E = 0$$

$\downarrow$   
 $= I_C$

$$R_C + R_E = \frac{V_{CC} - V_{CE}}{I_C}$$

$$= \frac{12 - 6}{1.5} = 4k\Omega$$

$$\left\{ V_{CE} = \frac{V_{CC}}{2} \text{ (OR) } V_{CC} = 2V_{CE} \right\}$$

Select  $R_C > 2R_E$

Let  $R_C = 2.8 \text{ k } \Omega$

$R_E = 1.2 \text{ k } \Omega$

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**Step 3:** calculate  $R_{th}$  by using stability factor value.

$$S = \frac{1 + \beta}{1 + \frac{\beta R_E}{R_{Th} + R_E}}$$

$$S = \frac{101}{1 + \frac{100 \times 1.2}{R_{Th} + 1.2}} = 8$$

$$R_{Th} = 9.12 \text{ k } \Omega = R_B$$

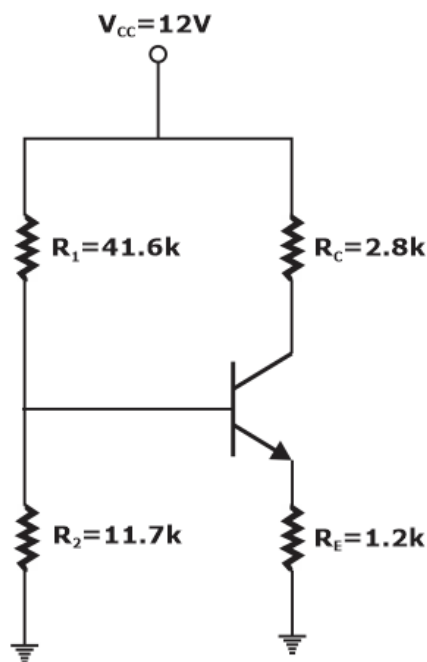
**Step 4:** Calculate  $V_{th}$  by using KVC in base loop

$$V_{Th} = R_B \cdot I_B + V_{BE} + I_E \cdot R_E$$

$$= \frac{1.5}{100} \times 9.12 + 0.7 + 1.5 \times 1.2$$

$$V_{Th} = 2.63 \text{ volt}$$

**Step 5:** Calculate  $R_1$  &  $R_2$



$$\frac{R_{Th}}{V_{Th}} = \frac{\frac{R_1 R_2}{R_1 + R_2}}{\frac{V_{CC} R_2}{R_1 + R_2}} = \frac{R_1}{V_{CC}}$$

$$R_1 = \frac{V_{CC}}{V_{Th}} \times R_{Th}$$

$$= \frac{12}{2.63} \times 9.12$$

$$R_1 = 41.61 \text{ k } \Omega$$

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$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} \Rightarrow R_2 = \frac{R_{Th} R_1}{R_1 - R_{Th}}$$

$$R_2 = 11.7 \text{ k } \Omega$$

**Note:** If stability factor value is not provided then  $R_{Th}$  is calculated by using the condition

$$(1 + \beta) R_E \gg R_{Th}$$

$$\text{Take } (1 + \beta) R_E = 10R_{Th}$$

$$R_{Th} = \frac{(1 + \beta)}{10} R_E$$

Thus  $R_1 = 41.61 \text{ k } \Omega$ ,  $R_2 = 11.7 \text{ k } \Omega$ ,  $V_{CC} = 12V$ ,  $R_C = 2.8 \text{ k } \Omega$ ,  $R_E = 1.2 \text{ k } \Omega$

\*\*\*\*



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