ISRO 2020 Computer Science & Engineering

Mega Mock Challenge
(08 Jan-09 Jan 2020)

Questions & Solutions

1. The most efficient algorithm for finding the number of connected components in an undirected graph on n vertices and *m* edges has time complexity
   A. Θ(n)   B. Θ(m)
   C. Θ(m+n)   D. Θ(m n)

Ans. C

Sol. The signal source shortest paths algorithm like Dijkstra algorithm find the shortest path to connect nodes in a graph on m vertices and n edges has time complexity Θ(m+n).

2. What is recurrence relation for the worst case of Quicksort and time complexity in the Worst case of Quick Sort respectively?
   A. $T(n) = T(n-2) + O(1)$ and $O(n^2)$
   B. $T(n) = T(n-1) + O(n)$ and $O(n^2)$
   C. $T(n) = 2T(n/2) + O(n)$ and $O(n \log n)$
   D. $T(n) = T(n/10) + T(9n/10) + O(n)$ and $O(n \log n)$

Ans. B

Sol. The worst case of Quick sort occurs when the pivot is chosen as first (last) element from the given elements of sorted array.
   In worst case, Quick sort recursively calls one sub problem with size 0 and other sub problem with size (n-1).
   So recurrence is $T(n) = T(n-1) + T(0) + O(n)$
   Time complexity is $O(n^2)$

3. Group 1 contains some CPU scheduling algorithms and Group 2 contains some applications. Match entries in Group 1 to entries in Group 2.

Group I	Group II
(P) Gang Scheduling	(1) Guaranteed Scheduling
(Q) Rate Monotonic Scheduling	(2) Real–time Scheduling
(R) Fair Share Scheduling	(3) Thread Scheduling

   A. P – 3 Q – 2 R – 1
   B. P – 1 Q – 2 R – 3
   C. P – 2 Q – 3 R – 1
   D. P – 1 Q – 3 R – 2

Ans. A

Sol. Gang scheduling for parallel systems that schedules related threads or processes to run simultaneously on different processors

Rate monotonic scheduling is used in real–time operating systems with a static–priority scheduling class. The static priorities are assigned on the basis of the cycle duration of the job: the shorter the cycle duration is, the higher is the job's priority.
Fair Share Scheduling is a scheduling strategy in which the CPU usage is equally distributed among system users or groups, as opposed to equal distribution among processes. It is also known as guaranteed scheduling.
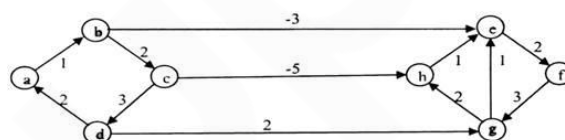
4.
   Dijkstra's single source shortest path algorithm when run from vertex 'a' in the above graph, computes the correct shortest path distance to
   A. only vertex a
   B. only vertices a, e, f, g, h
   C. only vertices a, b, c, d
   D. all the vertices

Ans. D

Sol. Dijkstra's single source shortest path is not guaranteed to work for graphs with negative weight edges, but Dijkstra's algorithm gives correct solution for the given graph. So, it computes correct shortest paths to all vertices.

5. In the following process state transition diagram for a uniprocessor system, assume that there are always some processes in the ready state:
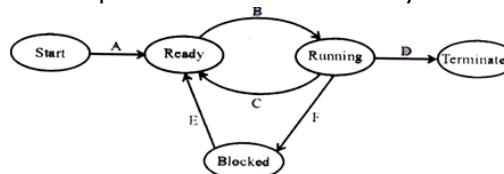
Now consider the following statements:
I. If a process makes a transition D, it would result in another process making transition A immediately.
II. A process P2 in blocked state can make transition E while another process P1 is in running state.

III. The OS uses preemptive scheduling.

IV. The OS uses non-preemptive scheduling. Which of the above statements are TRUE?

A. I and II B. I and III

C. II and III D. II and IV

Ans. C

Sol. In preemptive scheduling the process which allocated the CPU keeps it and release it only when it switching to waiting state. Also a process P_2 in blocked state can make transition E while other process P_1 in running **Alternately**

A process P_2 in blocked state can make transition E while another P_1 is in running state.

The OS uses preemptive Scheduling.

6. Let R and S be relational schemes such that R = {a, b, c} and S = {c}. Now consider the following queries on the Database:

I. $\pi_{R-S}(r) - \pi_{R-S}(\pi_{R-S}(r) \times s - \pi_{R-S,s}(r))$

II. $\{t \mid t \in \pi_{R-s}(r) \wedge \forall u \in s(\exists v \in r(u=v[s] \wedge t=v[R-S]))\}$

III. $\{t \mid t \in \pi_{R-s}(r) \wedge \forall v \in r(\exists u \in s(u=v[s] \wedge t=v[R-S]))\}$

IV. Select *R.a, R.b*

from *R, S*

where *R.c = S .c*

Which of the above queries are equivalent?

A. I and II B. I and III

C. II and IV D. III and IV

Ans. A

Sol. Query ! and 2 are equivalent since query 2 is the tuple alzebra for division operator and Query 1 is the realtional alzebra for division operator. whereas, Query 3 calculates the natural join of R & S.

7. A multilevel page table is preferred in comparison to a single level page table for translating virtual address to Physical address because

A. It reduces the memory access time to read or write a memory location.

B. It helps to reduce the size of page table needed to implement the virtual address space of a process.

C. It is required by the translation look a side buffer.

D. It helps to reduce the number of page faults in page replacement algorithms.

Ans. B

Sol. Most computer system supports a large logical address space (2^{32} to 2^{64}). The page table becomes excessively large for example. Consider a system with a 32 bit logical address space. If page size 4K (2^{12}) then page table may consist 1 million pages. For this we use multi levels page table.

8. The minimum number of comparisons required to determine if an integer appears more than n/2 times in a sorted array of n integers is

A. $\Theta(n)$ B. $\Theta(\log n)$

C. $\Theta(\log^* n)$ D. $\Theta(1)$

Ans. B

Sol. 1) locate middle element, if an element appears more than n/2 times, it will present at middle: O(1)

2) Find the starting position of an element which is same as middle (if repeats) : O(log n)

3) Find the ending position of an element which is same as middle (if repeats) : O(log n)

4) just compare starting and ending locations of an array : O(1)

So requires O(log n) time.

9. In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$P_i = A_i \oplus B_i$ and $G_i = A_i B_i$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look-ahead carry adder are given by:

$S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_i C_i$,

where C_0 is the input carry. Consider a two-level logic implementation of the look-ahead carry generator. Assume that all i and G i P are available for the carry

generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively:

A. 6, 3   B. 10, 4
C. 6, 4   D. 10, 5

Ans. B

Sol. Four number of carries are needed to design CLG
For C1 one AND gate + one OR gate
For C2 tow AND gates + one OR gate
For C3 three AND gates + one OR gate
For CA four AND gates + one OR gate
So total ten AND gates are needed and four OR gates are needed

10. It is observed that in unweighted graph, shortest path from node S to every node is calculated in terms of time complexity. So, by which of the following process, time complexity can be obtained?
A. Dijkstra's algorithm starting from S.
B. Warshall's algorithm
C. Performing a DFS starting from S.
D. Performing a BFS starting from S.

Ans. D

Sol. Breadth-first search is a way to visit all nodes at same distance from starting node before visiting farther nodes. It is also used to find all nodes reachable from starting node which serves as a shortest path between two nodes in an unweighted graph.
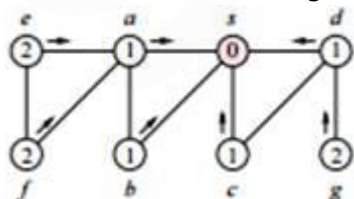
It is assumed that the BFS can be used for unweighted graphs, so time complexity will be $O(|E| + |V|)$

11. The program is executed from Main Memoryuntil it attempts to reference a page that is still in auxiliary memory, this condition is called as _____

A. Page Replace   B. Page Fault
C. Page Hit   D. Page Miss

Ans. B

Sol. The program is executed from Main Memoryuntil it attempts to reference a page that is still in auxiliary memory; this condition is called as Page Fault.

12. The database of Students_Records is shown in the table.

Student Class Fees
Rohit 5 10000.00
Sonu 6 5000.00
Mudit 5 10000.00

Find the output of the SQL query?
SELECT Count(*)
FROM ((SELECT Student, Class
FROM Students_Records) AS A
NATURAL JOIN (SELECT Class, Fees
FROM Students_Records) AS B);

A. 3   B. 9
C. 5   D. 6

Ans. C

Sol. We see that the content of temporary table A is shown:
Student Class
Rohit 5
Sonu 6
Mudit 5

We see that the content of temporary table B is shown:
Class Fees
5 10000.00
6 5000.00
5 10000.00

If we combine the tables A and B, we see that the natural join of two tables. If is found that the natural join appears on column name with the same name which is Class as shown. It is noted that 5 appears two times in the Class column, so there will be four entries with Class as 5.

Students Class Fees
Rohit 5 10000.00
Rohit 5 10000.00
Sonu 6 5000.00
Mudit 5 10000.00
Mudit 5 10000.00

13. Which is incorrect about Normal Forms?
    A. BCNF is stricter than 3NF
    B. There exists no redundancy in 3NF
    C. There exists dependency that preserve decomposition in BCNF
    D. The decomposition exist as lossless if there exists no loss in information by changing relations

Ans. B

Sol. We say that the decomposition is a lossless decomposition if there is no loss of information by replacing r (R) with two relation schemas r1(R1) andr2(R2). The reasons to select 3NF or BCNF have to do with how redundancy free you want to be. In BCNF there will be no more redundancy as can be caused by functional dependencies. In 3NF such redundancy can still occur.

14. Consider a paging hardware with a TLB. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6, the effective memory access time (in milliseconds) is _____.
    A. 118   B. 120
    C. 122   D. 124

Ans. C

Sol. $T_{ave} = H_1 \times (T_{TLB} + T_M) + (1-H_1) \times (T_{TLB} + 2 \times T_M)$
    T_{TLB} = time to search in TLB = l0 ms
    T_M = time to access physical memory = 30 ms
    H_1 = TLB hit ratio = 0.6
    $T_{ave} = 0.6 \times (I0+80) + (1 - 0.6) (10 + 2 \times 80)$
    $T_{ave} = 0.6 \times 90ms + 0.4(170)ms$
    $T_{ave} = 54ms + 68ms = 122ms$

15. A system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (LRU) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string given below?
    4, 7, 6, 1, 7, 6, 1, 2, 7, 2
    A. 4   B. 5
    C. 6   D. 7

Ans. C

Sol. What is a Page fault? An interrupt that occurs when a program requests data that is not currently in real memory. The interrupt triggers the operating system to fetch the data from a virtual memory and load it into RAM. Now, 4, 7, 6, 1, 7, 6, 1, 2, 7, 2 is the reference string, you can think of it as data requests made by a program. Now the system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (LRU) page replacement policy.
[ ] - Initially page frames are empty. i.e. no process pages in main memory.
[4] - Now 4 is brought into 1st frame (1st page fault)
Explanation: Process page 4 was requested by the program, but it was not in the main memory (in form of page frames), which resulted in a page fault, after that process page 4 was brought in the main memory by the operating system.
[4 7] - Now 7 is brought into 2nd frame (2nd page fault) - Same explanation.
[4 7 6] - Now 6 is brought into 3rd frame (3rd page fault)
[1 7 6] - Now 1 is brought into 1st frame, as 1st frame was least recently used (4th page fault). After this 7, 6 and 1 are were already present in the frames hence no replacements in pages.
[1 2 6] - Now 2 is brought into 2nd frame, as 2nd frame was least recently used (5th page fault).
[1 2 7] -Now 7 is brought into 3rd frame, as 3rd frame was least recently used (6th page fault).
Hence, total number of page faults(also called pf) are 6. Therefore, C is the answer.

16. Which one of the following is FALSE?
    A. User level threads are not scheduled by the kernel.
    B. When a user level thread is blocked, all other threads of its process are blocked.
    C. Context switching between user level threads is faster than context switching between kernel level threads.
    D. Kernel level threads cannot share the code segment.

Ans. D

Sol. From the given options, it is clear that, statement D is False because Kernel level threads within the same process can share code section.

17. The amount of ROM needed to implement a 4 bit multiplier is
    A. 64 bits   B. 128 bits
    C. 1 Kbits   D. 2 Kbits

Ans. D

Sol. For a 4 bit multiplier there are $2^4 \times 2^4 = 2^8 = 256$ combinations
    Output will contain 8 bits.
    So the amount of ROM needed is $2^8 \times 8$ bits = 2 Kbits.

18. The grammar S → aSa | bS | c is
    A. LL(1) but not LR(1)
    B. LR(1) but not LR(1)
    C. Both LL(1) and LR(1)
    D. Neither LL(1) nor LR(1)

Ans. C

Sol. It is LL (1) and LR(1)
    Given grammar:
    S → aSa
    S → bS
    S → c
    LL(1) table:

S	a	b	c
	s→aSa	s→bS	s→c

no multiple production in any entry.
so it is LL(1) grammar.
Every LL(1) Grammar is LR (1) grammar .
Hence, it is both LL(1) and LR(1)

19. A computer system supports 32-bit virtual addresses as well as 32-bit physical addresses. Since the virtual address space is of the same size as the physical address space, the operating system designers decide to get rid of the virtual memory entirely. Which one of the following is true?
    A. Efficient implementation of multi-user support is no longer possible
    B. The processor cache organization can be made more efficient now
    C. Hardware support for memory management is no longer needed
    D. CPU scheduling can be made more efficient now

Ans. C

Sol. We need a hardware support from memory management for supporting virtual. As the System designers decide to get rid of the virtual memory hence there is no need of hardware support.

20. A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:
    A. 1.0 second   B. 1.2 seconds
    C. 1.4 seconds   D. 1.6 seconds

Ans. C

Sol. Given, Delay at third stage = 2 slots
    Total instructions = 10^9
    Number of conditional branches = 20% of 10^9
    We know that cycle penalty = delay × conditional branches
    = 2 x 0.2 x 10^9= 4 x 10^8
    Also it is mention as the clock speed is 1 GHz
    So total execution
    time $= \dfrac{10^9}{10^9} + 4 \times \dfrac{10^8}{10^9}$ = 1.4 seconds

21. For S ∈ (0 + 1) * let d(s) denote the decimal value of s (e.g. d(101) = 5).

Let L = {s ∈ (0 + 1)* d(s)mod5 = 2 and d(s)mod7 != 4}.
Which one of the following statements is true?
A. L is recursively enumerable, but not recursive
B. L is recursive, but not context-free
C. L is context-free, but not regular
D. L is regular

Ans. D

Sol. It is regular
L1=d(s) mod 5 =2 is regular with 5 states
L2=d(s) mod 7 =4 is regular with 7 states
therefore L1 ^ L2' should be regular because regular grammar are closed under intersection and compliment

22. The following are the starting and ending times of activities A, B, C, D, E, F, G and H respectively in chronological order:
"as bs cs ae ds ce es fs be
de gs ee fe hs ge he".
Here, xs denotes the starting time and xe denotes the ending time of activity X. We need to schedule the activities in a set of rooms available to us. An activity can be scheduled in a room only if the room is reserved for the activity for its entire duration. What is the minimum number of rooms required?
A. 3   B. 4
C. 5   D. 6

Ans. B

Sol. Maximum room required = 4
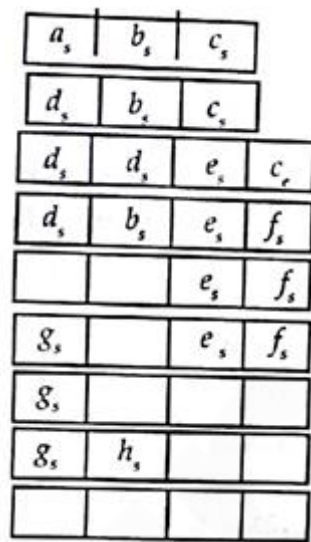
a_e is finish from room
entry of a_s in place of a_e in room
c_s is out and e_s in available room
f_s is in next room
b_e and d_e are vacant due to end
g_s is start in available room
e_e and f_e vacant the room
h_s is start in vacant room
all vacant room.

23. Consider two languages L1 and L2, each on the alphabet Σ. Let f: Σ → Σ be a polynomial time computable bijection such that (∀x)[x∈ L1 iff f(x) ∈L2]. Further, let f⁻¹ be also polynomial time computable. Which of the following CANNOT be true?
A. L1 ∈ P and L2 is finite
B. L1 ∈NP and L2 ∈ P
C. L1 is undecidable and L2 is decidable
D. L1 is recursively enumerable and L2 is recursive

Ans. C

Sol. We have one to one mapping for all instances of L1 to L2.
L1 is given to be undecidable.
Further L1 is polynomial time reducible to L2. (By given mapping).
Now if L2 is decidable then there is algorithm to solve L2 in polytime.
But then we can solve every instance of L1 in poly time, making L1 also decidable. Contradiction

24. Let G = ({S},{a,b},R,S) be a context free grammar where the rule set R is
S → a S b | S S | ε
Which of the following statements is true?
A. G is not ambiguous
B. There exist x, y ∈ L(G) such that xy∉L(G)
C. There is a deterministic pushdown automaton that accepts L(G)
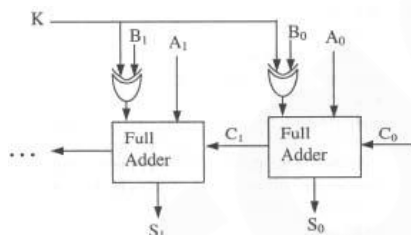D. We can find a deterministic finite state automaton that accepts L(G)

Ans. C
Sol.
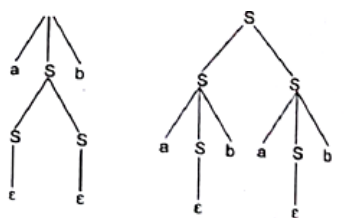
$S \rightarrow aSb \mid SS \mid \in$

Hence, S is ambiguous
Langauge generated by given grammar is $(a^n b^n)^*$
So, we can find a deterministic push down automation that accepts L(G).

25. Consider the ALU shown below.

If the operands are in 2's complement representation, which of the following operations can be perforModerate by suitably setting the control lines K and C0 only (+ and – denote addition and subtraction respectively)?
A. A + B, and A - B, but not A + 1
B. A + B, and A + 1, but not A – B
C. A + B, but not A – B or A + 1
D. A + B, and A - B, and A + 1

Ans. A
Sol.
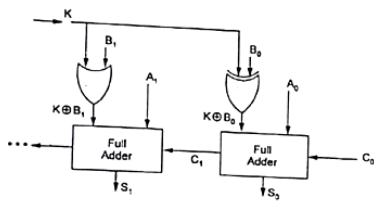
If $k = 1$, $C_0 = 1$
$$S_0 = \overline{B_0} \oplus A_0 \oplus C_0 = \overline{B_0} \oplus \overline{A_0}$$
$$= A_0 \overline{B_0} + B_0 \overline{A_0}$$
$$C = \overline{B_0} A_0 + (\overline{B_0} \oplus A_0) C_0$$
$$= \overline{B_0} A_0 + B_0 A_0 + \overline{A_0} \overline{B_0}$$
$$= A_0 + \overline{A_0} \overline{B_0}$$
$$S = A_1 \oplus \overline{B_1} \oplus C_1$$
If $k = 0$, $C_0 = 1$
$$S_0 = A_0 \oplus \overline{B_0} \oplus 1 = A_0 \oplus \overline{B_0}$$
$$= A_0 B_0 + \overline{A_0} \overline{B_0}$$
$$C = A_0 B_0 + (A_0 \oplus B_0) = A_0 + \overline{A_0} \overline{B_0}$$
= A+B and A-B but not A - 1

26. Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Instruction	Operation	Instruction Size (in words)
MOV R1,5000	;R1 ← Memory[5000]	2
MOV R2(R1)	;R2 ← Memory[(R1)]	1
ADD R2, R3	;R2 ← R2 + R3	1
MOV 6000, R2	; Memory[6000] ← R2	2
HALT	;Machine halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting form memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be
A. 1007   B. 1020
C. 1024   D. 1028

Ans. D
Sol. Instruction size are given in words. So first instruction will take 2 words i.e 8 bytes(as 32 bit byte addressable, word size will be 32 bit) so on for 2nd instruction 4 byte, for 3rd 4 bytes, 4th 8 bytes.5th 4 bytes. As 1st instruction starts from 1000 and the size is 8 bytes second instruction address will be 1008, likewise 3rd instruction address will be 1012,4th instruction address 1016,5th instruction address 1024 and halt instruction address will be 1028. Word size is 32 bits (4 bytes). Interrupt occurs after

execution of HALT instruction NOT **during**, So address of next instruction will be saved on to the stack which is 1028.

27. The minimum number of page frames that must be allocated to a running process in a virtual memory environment is determined by
A. the instruction set architecture
B. page size
C. physical memory size
D. number of processes in memory

Ans. A

Sol. There are two important tasks in virtual memory management: a page-replacement strategy and a frame-allocation strategy. Frame allocation strategy says gives the idea of a minimum number of frames which should be allocated. The absolute minimum number of frames that a process must be allocated is dependent on system architecture, and corresponds to the number of pages that could be touched by a single (machine) instruction. So, it is instruction set architecture i.e. option (A) is correct answer.

28. Consider a disk drive with the following specifications:
16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is
A. 10   B. 25
C. 40   D. 50

Ans. B

Sol. Direct memory access (DMA) is a feature of computer systems that allows certain hardware subsystems to access main system memory (RAM) independently of the central processing unit (CPU). Without DMA, when the CPU is using programmed input/output, it is typically fully occupied for the entire duration of the read or write operation, and is thus unavailable to perform other work.
Time takes for 1 rotation = 60/3000
It reads 512*1024 Bytes in one rotation.
Time taken to read 4 bytes = 153 ns
153 is approximately 4 cycles (160ns)
Percentage of time CPU gets blocked = 40*100/160 = 25

29. What is the swap space in the disk used for?
A. Saving temporary html pages
B. Saving process data
C. Storing the super-block
D. Storing device drivers

Ans. B

Sol. Swap space is typically used to store process data. Swap space in Linux is used when the amount of physical memory (RAM) is full. If the system needs more memory resources and the RAM is full, inactive pages in memory are moved to the swap space. While swap space can help machines with a small amount of RAM, it should not be considered a replacement for more RAM. Swap space is located on hard drives, which have a slower access time than physical memory. Swap space can be a dedicated swap partition (recommended), a swap file, or a combination of swap partitions and swap files. Swap should equal 2x physical RAM for up to 2 GB of physical RAM, and then an additional 1x physical RAM for any amount above 2 GB, but never less than 32 MB.

30. An example of a spooled device is
A. A graphical display device
B. A line printer used to print the output of a number of jobs
C. A secondary storage device in a virtual memory system
D. A terminal used to enter input data to a running

Ans. B

Sol. A spooled device is the one that quess the spool of printer jobs and takes one job at a time and prints the output.

31. What is the purpose of DMA facility in microprocessor based system?
    A. To increase the speed of data transfer between the microprocessor and I/O devices.
    B. To increase the speed of data transfer between the μP and the memory.
    C. To increase the speed of data transfer between the memory and the I/O devices.
    D. To improve the reliability of the system

Ans. C

Sol. In DMA (Direct Memory Access) scheme, data are directly transferred from on I/O device to or from RAM to I/O device. The microprocessor has to relinquish the control of the address and data buses for DMA operation on the request of I/O device. Thus the speed increases in DMA operation.

32. Which of the following are the memory performance parameters?
    1). Access time and latency
    2). Block size and Block access time
    3). Cycle time and Bandwidth
    Select the correct answer from the codes given below:
    A. 1 only   B. 1 and 2 only
    C. 2 and 3 only   D. 1, 2 and 3

Ans. D

Sol. All are memory performance parameters.

33. A magnetic drum of 8 inch diameter has 100 tracks and storage density of 200 bits/inch. What is its storage capacity?
    A. 8402 bits   B. 202400 bits
    C. 502400 bits   D. 1004800 bits

Ans. C

Sol. Storage capacity
$= \pi \times diameter \times tracks \times storage\, density$
$= 3.14 \times 8 \times 100 \times 200 = 502400\, bits$

34. A memory system of size 16 Kbytes is required to be designed using memory chips which have 12 address lines and 4 data lines each. What is the number of such chips required to design the memory system?

A. 2   B. 4
C. 8   D. 16

Ans. C

Sol. Number of chips
required $= \dfrac{16 \times 2^{10} \times 8}{2^{12} \times 4} = 8$

35. **Statement (I):** The data path contains all the circuits to process data within the CPU with the help of which data is suitably transformed.
    Statement (II): It is the responsibility of the control path to generate control and timing signals as required by the op code.
    A. Both Statements (I) and Statements (II) are individually true and Statements (II) is the correct explanation of Statements (I).
    B. Both Statements (I) and Statements (II) are individually true but Statements (II) in not the correct explanation of Statements (I).
    C. Statement (I) is true but Statements (II) is false.
   D. Statement (I) is false but Statement (II) is true.

Ans. A

Sol. The control unit tells the data path what to do, based on the instruction that is currently being executed. The control unit sets the data path signals appropriately so that registers are read, ALU output is generated, data memory is read or written and branch target addresses are computer.

36. What is maximum number of nodes in a binary tree that has N levels, if the root is at level zero?
    A. 2^{2N} B. $2^{N+1} - 1$
    C. $2^N - 1$ D. $2^N - 2N$

Ans. C

Sol. Number of levels = N
    A maximum number of nodes in a binary tree =?
    If N = 1 ⟹ 1 node in tree (only root)
    Note that level 0 only present means N=0 because a number of levels is 1.
    N = 2 ⟹ 3 node (maximum) in tree

N = 3 $\Rightarrow$ 7 node (maximum) in tree
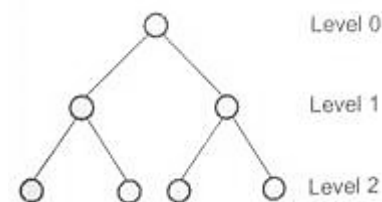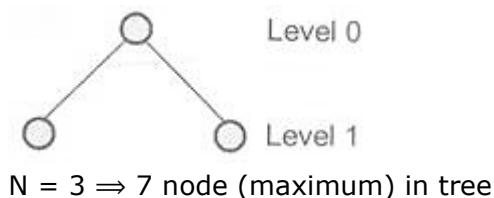
[**Note:** if number of levels is zero then no tree is possible]

∴ Maximum number of nodes in a binary tree

= $(2^N - 1)$

37. The data type defined by a user is.
   A. Built-in data type
   B. Abstract data type
   C. Homogeneous data type
   D. Real data type

Ans. B

Sol. The data type defined by a user is abstract data type. Abstract Data type (ADT) is a type (or class) for objects whose behavior is defined by a set of value and a set of operations. A **real data type** is a **data type** used in a computer program to represent an approximation of a **real** number. **Homogeneous data** structures are those **data** structures that contain the only similar **type** of **data** e.g. like a **data** structure containing only integer or float values. In most programming languages, all basic data types are built-in

38. How many distinct binary trees can be constructed with three nodes?
   A. 1   B. 2
   C. 3   D. 5

Ans. D

Sol. n# Distinct binary trees constructed with 3 nodes.

$$= \frac{^{2n}C_n}{n+1} = \frac{^6C_3}{4} = 5$$

39. Consider the following statements:
   1). Taking 2's complement is equivalent to sign change.
   2). In the 2's complement representation the most significant bit (MSB) is zero for a positive number.
   3). In a 4 bit binary representation of a binary number A, A + 1's complement of A = 2^4.
   Which of the above statements are correct?
   A. 1 and 2 only
   B. 1 and 3 only
   C. 2 and 3 only
   D. 1, 2 and 3

Ans. A

Sol. Taking 2's complement is equivalent to sign change. In the 2's complement representation the most significant bit (MSB) is zero for a positive number. The range of numbers possible in 2's complement for n-bits is -2^n. so option a is only correct.

40. Find number of equivalence classes for the following regular expression R?
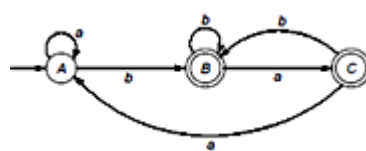   R= (a+b) * b (a+b+ε)
   A. 1   B. 2
   C. 3   D. 4

Ans. C

Sol. R= (a+b) * b (a+b+ε)

$$= (a+b)^* b + (a+b)^* bb + (a+b)^* ba$$

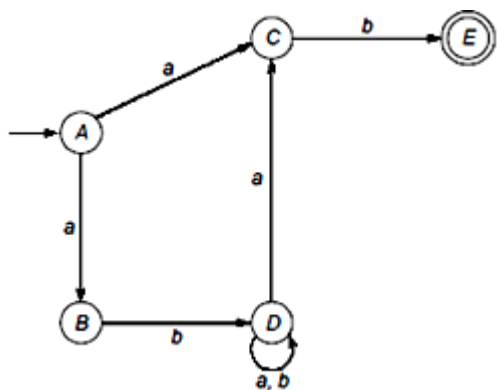$$= (a+b)^* b + (a+b)^* ba$$

Minimized DFA that accepts language generated by R.

$\Rightarrow$ 3 equivalence classes

∵ 3 states.

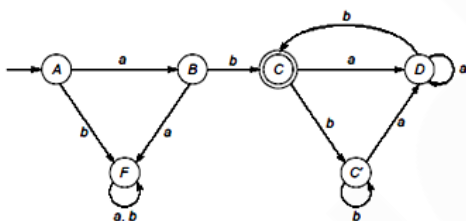41. Consider the following non-deterministic finite automata over

How many states in the minimized DFA which is equivalent to the above NFA?

A. 3 B. 6
C. 9 D. 10

Ans. B

Sol. Language accepted by the given NFA is all strings start and end with 'ab'.

ab + abXab

Equivalent DFA contain minimum 6 states.

42. Find the grammar that generates inherently ambiguous context free language.

A. $S \to AB \mid CD$
$A \to aAb \mid \varepsilon$
$B \to dB \mid \varepsilon$
$C \to aC \mid \varepsilon$
$D \to bDd \mid \varepsilon$

B. $S \to AB \mid CD$
$A \to aAb \mid \varepsilon$
$B \to bB \mid \varepsilon$
$C \to aC \mid bC \mid \varepsilon$
$D \to bB \mid \varepsilon$

C. Both A and B

D. Neither A nor B

Ans. C

Sol. Here option A and option B are ambiguous grammars. But Inherently ambiguous language definition not depends on given grammar type and it depends on language generated by given grammar.

So, Option A produces the following language:

$L = \{a^m b^n c^k \mid m = n \text{ or } n = k\}$

The above language has no equivalent unambiguous grammar. Because every grammar that generates the above language is always ambiguous grammar. So we call the above language is inherently ambiguous language.

Option B produces the following language:

$L = (a + b)^*$

Even though given option B is ambiguous grammar, the language is not inherenly ambiguous language. Because this language has equivalent unambiguous grammars in the world.

Option A is inherently ambiguous language, because no equivalent unambiguous grammar exist for the language.

Option B is not inherently ambiguous language, because many unambiguous grammars exist for the language.

43. Let L1 = 0*1*, L2=1*0*, L3=(0+1)*, and L4=0*1*0* .
Then find the number of strings in the following language L.
L= (L1 ∩ L2) - (L3 ∩ L4)

A. 0 B. 2
C. 5 D. 9

Ans. A

Sol.

$L_1 = 0^*1^*, L_2 = 0^*1^*$ $\Rightarrow L_1 \cap L_2 = 0^* + 1^*$
$L_3 = (0+1)^*, L_4 = 0^*1^*0^*$ $\Rightarrow L_3 \cap L_4 = (0+1)^*$
$\cap 0^*1^*0^* = 0^*1^*0^*$
$L = (L_1 \cap L_2) - (L_3 \cap L_4) = (0^* + 1^*) - (0^*1^*0^*) = \{\}$

∴ Zero number of strings in L.

44. Let L = $\{(a^p)^* \mid p$ is a prime number$\}$ and $\Sigma = \{a\}$. How many minimum number of states in NFA that accepts a language L?
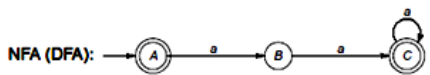
A. 1 B. 2
C. 3 D. 5

Ans. C

Sol.

$$L = \{(a^P)* \mid P \text{ is a prime}\}$$
$$= (a^2)* \cup (a^3)* \cup (a^5)* \cup \ldots$$
$$= \{\varepsilon, a^2, a^3, a^4, a^5, a^6, \ldots\}$$

= All strings of a's except the string a.

$$= \{a^n \mid n = 0 \text{ or } n \geq 2\}$$
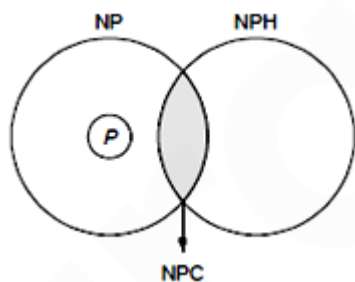
NFA (DFA):

Number of states = 3.

Note: a^{prime} is not regular but kleene closure of this language is regular.

45. Assume P represents class of P-problems, NP represents class of NP-problems, and NPC for class of NP-complete problems. Identify the correct relation from the following.
   A. $P \cap NPC = NPC$
   B. $P \cap NP = P$
   C. $NP \cap NPC = NP$
   D. $NP - P = NPC$
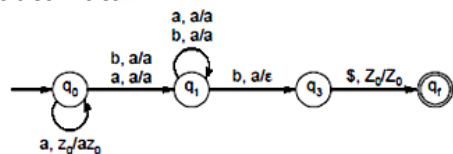
Ans. B

Sol.

(i) $P \cap NPC = \phi$

(ii) $P \cap NP = P$

(iii) $NP \cap NPC = NPC$

(iv) $NP - P \neq NPC$

∴ Option B. is correct.
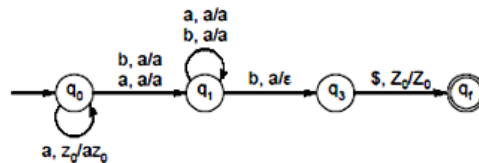
46. Consider the following push down automata.

The language accepted by above PDA is _____.
   A. Regular but infinite
   B. DCFL but not regular

C. CFL but not DCFL
D. Finite language.

Ans. A

Sol.

The language accepted by above PDA contain the strings where each string starts with 'a' and ends with 'b'. This language is regular.

47. Consider the following regular expression (RE).
   RE=(a+b)*(a+b+epsilon)a
   Which of the following is equivalent to the above RE?
   A. $(a * + b *) + (aa + ba)$
   B. (a+b)*a
   C. $(a + b) + (a + b + \varepsilon)a$
   D. None of these

Ans. B

Sol. $RE = (a + b) * (a + b + \varepsilon)a = (a + b) * a$

$(\varepsilon + a + b *) * a = (a + b) * a$

∴ Option B. is equivalent to given RE.

48. A machine has 24 bit instruction format. It has 32 registers and each of which is 32 bit long. It needs to support 49 instructions. Each instruction has two register operands and one immediate operand. If the immediate operand is signed integer, find the minimum value of immediate operand.
   A. (-122)   B. (-128)
   C. (-126)   D. (-121)

Ans. B

Sol.
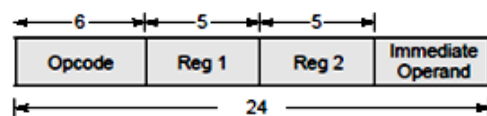
49 instructions ⇒ 6 bits needed for Op-code

32 registers ⇒ 5 bits needed for register operands

Immediate operand bits = 8

Minimum value $= -2^7 = -128$

49. Consider execution of 100 instructions on a 5 stage pipeline. Let P be the probability of an instruction being a branch. What must be the value of P such that speed up is atleast 4?

(Assume each stage takes 1 cycle to perform it's task and branch is predicted on fourth stage of the pipeline)

A. 0.3   B. 0.08
C. 0.27   D. .56

Ans. B

Sol.

$$\text{Speed up} = \frac{\text{Pipeline depth}}{(1 + \text{Branch frequency} \times \text{Branch penalty})} \geq 4$$

$$\frac{5}{1 + P \times 3} \geq 4$$

$$4 + 12P \leq 5$$

$$12P \leq 1$$

$$P \leq \frac{1}{12}$$

50. A 17 way set associative cache has 16 byte blocks and 32 bit byte addressable memory. The cache size is 17408 bytes. How many total bits required for both tag and word offset for any CPU reference?

A. 27   B. 26
C. 29   D. 30

Ans. B

Sol. 16 bytes per block, so there are $\log_2 16 = 4$ bits.

Cache size = 17408 bytes

$$\therefore \quad \frac{17408}{16} = 1088 \text{ blocks}$$

The cache is 17 way associative, so, there are $\frac{1088}{17} = 64$ sets

$\therefore \log_2 64 = 6$ bits (set number)

Number of tag bits is $32 - 6 - 4 = 22$ tag bits.

$22 + 4 = 26$

51. Suppose the cache memory is 100 times faster than main memory and it is used 50% of the time. How much performance is gained by introducing this cache?

A. 1.94   B. 2.01
C. 2.05   D. 1.98

Ans. D

Sol. Apply Amdhal's low

$S = 100$

$f = 50\%$

$$S_{overall} = \left[1 - 0.5 + \frac{0.5}{100}\right]^{-1}$$

$$= \left[0.5 + \frac{0.5}{100}\right]^{-1} = \left[\frac{101}{200}\right]^{-1}$$

$$= \frac{200}{101} = 1.98$$

52. Consider the following set of processes with the arrival times and burst times. Processes are scheduled using highest response ratio next.

Process	P_1	P_2	P_3	P_4
Arrival time	0	2	5	4
CPU burst time	4	1	2	2

What is the average waiting time of processes?

A. (0.25)   B. (1.25)
C. (2.25)   D. (3.25)

Ans. B

Sol. (i) At $t = 0$, P_1 will execute.

(ii) At $t = 4$, P_2 and P_4 are in ready queue.

$$RR_2 = \frac{2 + 1}{1} = 3$$

$$RR_4 = \frac{0 + 2}{2} = 1$$

$\therefore \quad P_2$ will execute (P_2 has highest RR)

(iii) At $t = 5$, P_4 and P_3 are in Ready queue

$$RR_4 = \frac{1 + 2}{2} = \frac{3}{2} = 1.5$$

$$RR_3 = \frac{0 + 5}{5} = 1$$

$\therefore \quad P_4$ will execute first, then P_3 will execute.

P_1	P_2	P_4	P_3
0 4	5	7	9

$WT_1 = 0$, $WT_2 = 4 - 2 = 2$

$WT_3 = 7 - 5 = 2$, $Wt_4 = 5 - 4 = 1$

Average waiting time

$$= \frac{0 + 2 + 2 + 1}{4} = \frac{5}{4} = 1.25$$

53. Match the following groups.
    Group-I (Scheduling)
    A- FCFS
    B- SJF
    C- Priority scheduling
    D- RR scheduling
    Group-II (Advantage)
    1- Used in time sharing system
    2- More reactive, used in real time system
    3- Minimizes average turn around time
    4- Very simple, next process can be selected quickly
    A. A-2, B-1, C-3, D-4
    B. A-4, B-3, C-2, D-1
    C. A-2, B-3, C-1, D-4
    D. A-4, B-2, C-3, D-1
Ans. B
Sol. **FCFS:** Very simple algorithm, selects next process quickly from queue.
    SJF: Minimizes average turnaround time.
    Priority scheduling: Used in real time system.
    RR: Used in time sharing system.

54. Consider the following components in a computer system
    C1:Computer Hardware
    C2:Application Programs
    C3:Utilities
    Find the place of operating system using the above components.
    A. Below C1
    B. In between C2 and C3
    C. In between C1 and C3
    D. None of the above
Ans. C
Sol.

Application Programs	C2
Utilities (System programs)	C3
Operating System	
Computer Hardware	C1

In between C1 and C3, OS is placed.

55. A relation R (A, B, C, D, E, F) holds following FDs.

$AB \rightarrow C$
$C \rightarrow D$
$D \rightarrow EA$
$E \rightarrow F$
$F \rightarrow B$

Find the number of minimal candidate keys of R.
    A. 2   B. 4
    C. 6   D. 8
Ans. A
Sol. Here candidate keys are AB, AE, AF, C, D
    Minimal candidate keys = C, D

56. Consider the following statements.
    (i) If relation R is in 3 NF and every key is simple then R is in BCNF
    (ii) If relation R is in 3 NF and R has only one key then R is in BCNF
    Which of the following is correct?
    A. Both (i) and (ii) true
    B. (i) is true and (ii) is false
    C. (i) is false and (ii) is true
    D. Both (i) and (ii) false
Ans. A
Sol. (i) If relation R is in 3 NF and every key is simple then R is in BCNF . It makes all FDs LHS have a key.
    (ii) If relation R is in 3 NF and R has only one key then R is in BCNF. Here also same that all FDs LHS will have the key.
    In both statements, relation has only functional dependencies where LHS of FD is a key, therefore the relation is in BCNF.

57. Consider a banking database with following relation loan(branchName, loan_no, amount)
    Find the loan number of each loan where an amount is greater than 10000.
    A. $\{t \mid t \in loans \wedge t[amount] > 10000\}$
    B. $\{t \mid \exists l \in loans(t[loan\_no]=l[loan\_no] \wedge l[amount] > 10000)\}$
    C. $\{t \mid \forall l \in loans(t[loan\_no]=l[loan\_no] \wedge l[amount] > 10000)\}$
    D. None of these
Ans. B
Sol. Option A. selects all the attribute of loan in the result.
    Option B. finds the loan number of

each loan where an amount is greater than 10000.

58. Consider 3 transactions T_1 T_2 and T_3 having 2, 3 and 4 operations respectively. Find number of concurrent schedules.
A. (1258)   B. (1259)
C. (1260)   D. (1265)

Ans. C

Sol. If T_1, T_2 and T_3 are transactions with p, q and r operations respectively

Number of concurrent schedules

$$= \frac{(p+q+r)!}{p!q!r!} = \frac{(2+3+4)!}{2!\,3!\,4!} = \frac{9!}{2 \times 6 \times 4!}$$

$$= \frac{9 \times 8 \times 7 \times 6 \times 5}{2 \times 6} = 63 \times 20$$

$$= 1260$$

59. **Identify the capabilities of SELECT statement.**
A. Projection
B. Selection
C. Data Control
D. Transaction
A. A only
B. A, B, C only
C. A and C only
D. A and B only

Ans. D

Sol. **Answer: A, B.** The SELECT statement can be used for selection, projection and joining.

60. In a particular number system having base B.

$$\left(\sqrt{41}\right)_B = 5_{10}$$

The value of 'B' is _____.
A. 4   B. 6
C. 8   D. 9

Ans. B

Sol. Squaring both side, $\left(\sqrt{41}\right)^2 = (5)^2$

$$(41)_B = (25)_{10}$$

$$(4B+1)_{10} = (25)_{10}$$

$$\Rightarrow \qquad B = 6$$

61. The output Y in the circuit below is always '1' when
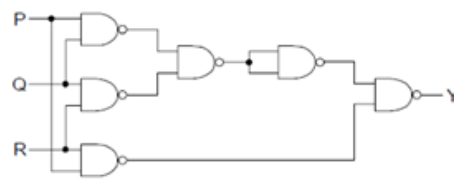
A. two or more of the inputs P,Q,R are '0'.
B. two or more of the inputs P,Q,R are '1'.
C. any odd number of the inputs P,Q,R is '0'
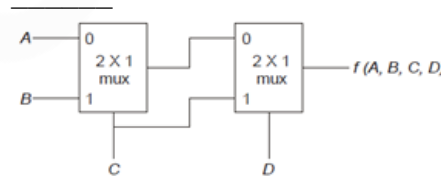D. any odd number of the inputs P,Q,R is '1'.

Ans. B

Sol. Take two or three input '1' then we always get '1'

Or

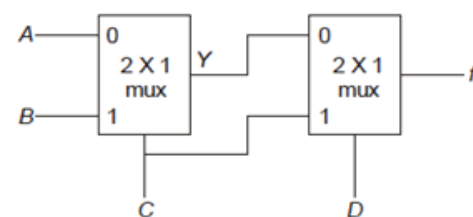Take two or three input ero then we always get '0' hence option 'b' is true and output Y=PQ+PR+RQ

62. Consider the logic circuit given below. The min terms in f(A,B,C,D) are _____

A. $\sum m\left(1,3,5,6,7,11,14\right)$

B. $\sum m\left(6,7,8,12,14,15\right)$

C. $\sum m\left(3,6,7,8,11,12,14,15\right)$

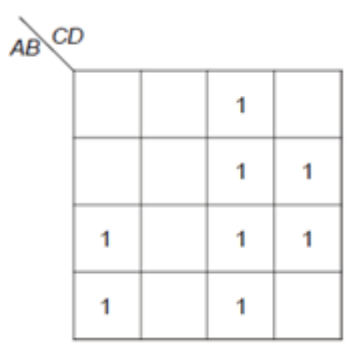D. $\sum m\left(3,6,7,9,11,12,14,15\right)$
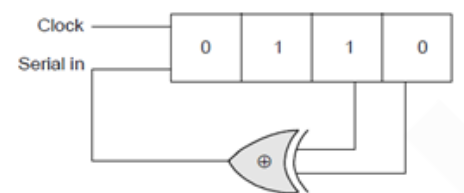
Ans. C

Sol.

$$Y = A\bar{C} + BC$$

$$f = Y\bar{D} + CD$$

$$f = \left(A\bar{C} + BC\right)\bar{D} + CD = A\bar{C}\bar{D} + BC\bar{D} + CD$$

$$f(A,B,C,D) = \sum m(3,6,7,8,11,12,14,15)$$

63. The initial contents of the 4-bit serial-in-parallel-out, right-shift, Shift Register shown in the figure is 0110. After three clock pulses are applied, the contents of the Shift Register will be
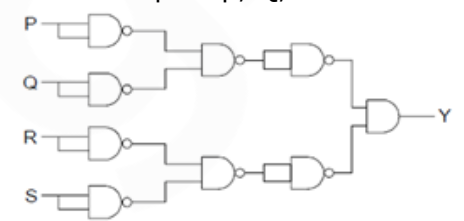

A. 0000   B. 0101

C. 1010   D. 1111

Ans. C

Sol.

	0	1	1	0
1st clk	1	0	1	1
2nd clk	0	1	0	1
3rd clk	1	0	1	0

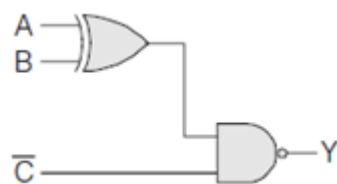64. For the circuit shown in figure the Boolean expression for the output Y in terms of inputs p, Q, R and S is

A. $\overline{P}+\overline{Q}+\overline{R}+\overline{S}$

B. P'Q'R'S'

C. $\left(\overline{P}+\overline{Q}\right)+\left(\overline{R}+\overline{S}\right)$

D. $(P+Q)(R+S)$

Ans. B

Sol. After 1st pass: P',Q',R',S'

After 2nd PASS: (P'Q')' , (R'S')'

After 3nd Pass: ((P'Q')' , (R'S')')'= P'Q'R'S'

65. The Boolean expression of the logic circuit shown in figure is

A. Y= AB'+A'B'+C

B. Y= AB + A'B'+C

C. Y= (AB)'+A'B'+C

D. Y= (AB)'+A'B'+C'

Ans. B

Sol.

$$Y = \overline{(A \oplus B).\overline{C}} = \overline{A \oplus B} + C$$

$$= A \odot B + C = AB + \overline{A}\overline{B} + C$$

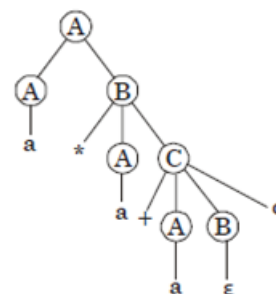66. Let G be the following grammar.

$$A-> AB/a$$

$$B-> *AC/Cb/\epsilon$$

$$C-> +ABc/\epsilon$$

Find the total number of reductions using LR(1) parser for the string a*a+ac using grammar G.

A. 7   B. 8

C. 9   D. 10

Ans. A

Sol. String = "a * a + ac"

# of reduction = # of intermediate nodes = # of substitution = 7 [reduction order in LR parser must be reverse of RMD]

67. Consider the following SDT.

E $\rightarrow$ E+T {E.x=E.x $\times$ T.x}

E $\rightarrow$ T {E.x=T.x}

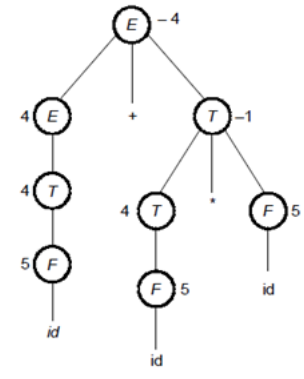T $\rightarrow$ T*F {T.x=T.x-F.x}

T $\rightarrow$ F {T.x=F.x-1}

$F \rightarrow$ id {F.x=5}

If bottom up parsing uses S-attributed definition then what is the value of attribute evaluated at root E for an input string " id+id*id "?

A. -4 B. -6
C. -8 D. -9

Ans. A

Sol. Input string "id+id*id"

The value -4 is computed at root E. (bottom up parsing uses " Reverse of RMD")

68. Consider the following CFG
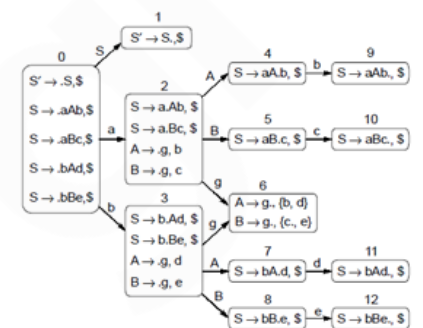$S \rightarrow$ aAb|aBc|bAd|bBe

$A \rightarrow$ g

$B \rightarrow$ g

How many states are exist in DFA using LALR (1) constructions for the above grammar?

A. 8 B. 10
C. 13 D. 15

Ans. C

Sol.

$\Rightarrow$ 13 state in DFA

69. Consider the C program
Main()
{
int x = 10;
x = x + y + z;
}

How many tokens are identified by lexical analyzer?

A. 18 B. 20
C. 23 D. 26

Ans. A

Sol. Y and z are not declared in the program and declaration error is produced by only semantic analyzer. Lexical analyzer job is to group the characters into a token.

Main ( )
{
int x = 10 ;
x = x + y + z ;
}

70. Consider the following grammar G.
$S \rightarrow$ AB|d
$A \rightarrow$ aA|b
$B \rightarrow$ bB|c

The grammar G is
A. LL (1) grammar and not LR (0)
B. LL (1) and LR (0)
C. Not LL (1) but LR (0)
D. Neither LL (1) nor LR (0)

Ans. B

Sol.
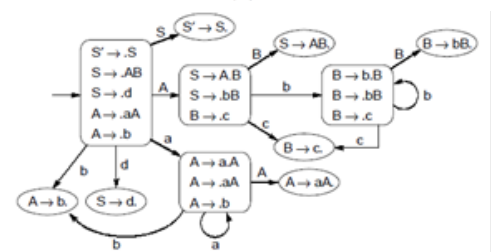
$S \rightarrow AB \mid d \Rightarrow Fi(AB) \cap Fi(d) = \phi$

$A \rightarrow aA \mid b \Rightarrow Fi(aA) \cap Fi(b) = \phi$

$B \rightarrow bB \mid c \Rightarrow Fi(bB) \cap Fi(c) = \phi$

$\Rightarrow Grammar\ is\ LL(1)$

No conflicts in above DFA of LR (0) parser.

$\therefore$ Grammar is LR(0)

$\Rightarrow$ Grammar G is both LL(1) and LR (0).

71. Which of the following can be used in syntax analysis to verify the syntax of programs?
A. Finite automata
B. Push down automata
C. Regular grammar
D. None of these

Ans. B

Sol. Push down automata can be used in syntax analysis to parse input string. Bottom up parsers and top down parser uses stack which works similar to PDA.

72. 'DOS' floppy disk does not have:
A. A boot record
B. A file allocation table
C. A root directory
D. virtual memory

Ans. D

Sol. virtual memory

73. The first page of a web site is called ____.
A. Homepage   B. Index
C. JavaScript   D. Bookmarks

Ans. A

Sol. The first page of a website is called Homepage.

74. The OSI model is divided into _____ processes called layers.
A. five   B. six
C. seven   D. eight

Ans. C

Sol. The Open System Interconnection (OSI) model defines a networking framework to implement protocols in seven layers. In the OSI model, control is passed from one layer to the next, starting at the application layer in one station, and proceeding to the bottom layer, over the channel to the next station and back up the hierarchy.

75. We can make a class abstract by
A. Declaring it abstract using the virtual keyword
B. Making at least one member function as virtual function
C. Making at least one member function as pure virtual function
D. Making all member function const.

Ans. C

Sol. A pure virtual function or abstract function in C++ is a virtual function for which we don't have any implementation, we can only declare it......
A pure virtual function is implemented by classes which are derived from a abstract class. Classes derived from the abstract class must implement the pure virtual function or they, too, are abstract classes

76. In C, after executing the following code what are the values of x, y and z?
int x,y = 10, z = 12;
x = y++ + z++;
A. x = 22, y=10, z=12
B. x = 22, y=11, z=13
C. x = 24, y=11, z=13
D. x = 22, y=11, z=14

Ans. B

Sol. From first equation
x=y++ +x++
x=10+12=22
then z++=13
&y=11
Therefore, the answer is x = 22, y=11, z=13

77. Out of the following life cycle models which one can be considered as the most general model, and the others as specialization of it?
A. Classical Waterfall Model
B. Iterative Waterfall Model
C. Prototyping Model
D. Spiral Model

Ans. A

Sol. Classical waterfall model is most general model among other models.

78. Which development phase in classical waterfall life cycle immediately follows coding phase?
A. Design
B. Maintenance
C. Testing
D. Requirement analysis and specification

Ans. C

Sol. The following order used in the development phase of waterfall software life cycle.
• Analysis
• Design
• Coding
• Testing
Testing is next phase after the coding.

79. Which one of the following phases is the last development phase of a classical waterfall software life cycle?

A. Design   B. Analysis
C. Testing   D. Coding

Ans. C

Sol. The following order used in the development phase of waterfall software life cycle.
- Analysis
- Design
- Coding
- Testing

Here, Testing is the last phase.

80. In the classical waterfall model during which phase is the Software Requirement Specification (SRS) document produced?
A. Design
B. Maintenance
C. Requirements analysis and specification
D. Coding

Ans. C

Sol. The document which contains all this information is called SRS, and it clearly and unambiguously indicates the requirements. A small amount of top-level analysis and design is also documented. This document is verified and endorsed by the customer before starting the project. SRS serves as the input for further phases. Software Requirements analysis (SRS) document produced during requirements analysis and specification.

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